Applications, Techniques and Procedures for Digital-Computer Control of Army Vibration Testing Sine Sweep/Dwell Tests

September 1975

U.S. Army Materiel Command
HARRY DIAMOND LABORATORIES
Adelphi, Maryland 20783

UNCLASSIFIED
SECURITY CLASSIFICATION OF THIS PAGE (When Data Entered)

REPORT DOCUMENTATION PAGE		READ INSTRUCTIONS BEFORE COMPLETING FORM
1. REPORT NUMBER HDL-TR-1665	2. GOVT ACCESSION NO.	3. RECIPIENT'S CATALOG NUMBER
4. TITLE (and Subtitle) Applications, Techniques and Procedures for Digital-Computer Control of Army Vibration Testing Sine Sweep/Dwell Tests		5. TYPE OF REPORT & PERIOD COVERED Technical Report 6. PERFORMING ORG. REPORT NUMBER
7. AUTHOR(s) Abraham M. Frydman		8. CONTRACT OR GRANT NUMBER(s)
9. PERFORMING ORGANIZATION NAME AND ADDRESS Harry Diamond Laboratories 2800 Powder Mill Road Adelphi, MD 20783		10. PROGRAM ELEMENT, PROJECT, TASK AREA & WORK UNIT NUMBERS Prog Ele: 8L-3-P6350-01-AW-A9
11. CONTROLLING OFFICE NAME AND ADDRESS Army Materials & Mechanics Research Ctr. Watertown, MA 02172		12. REPORT DATE September 1975 13. NUMBER OF PAGES 182
14. MONITORING AGENCY NAME & ADDRESS(if different from Controlling Office)		15. SECURITY CLASS. (of this report) UNCLASSIFIED 15a. DECLASSIFICATION/DOWNGRADING SCHEDULE

16. DISTRIBUTION STATEMENT (of this Report)

Approved for Public Release; Distribution Unlimited.

This project has been accomplished as part of the U.S. Army Materials Testing Technology Program, which has for its objective the timely establishment of testing techniques, procedures, or prototype equipment (in mechanical, chemical, or non-destructive testing) to insure efficient inspection methods for materiel/material procured or maintained by AMC.

18. SUPPLEMENTARY NOTES

HDL Project No. 789385
AMCMS Code: 53960M6350

19. KEY WORDS (Continue on reverse side if necessary and identify by block number)

Shock and vibration testing
Direct-digital-computer control

20. ABSTRACT (Continue on reverse side if necessary and identify by block number)

The Harry Diamond Laboratories has been concerned with the establishment of reliable and cost-effective vibration-test techniques that are applicable to Army production and qualification testing. To further this goal, use was made of a new test method in which a digital mini-computer with associated peripherals assumes direct and full control of sinusoidal vibration testing. Replacing conventional analog test techniques,

DD FORM 1 JAN 73 1473 EDITION OF 1 NOV 65 IS OBSOLETE

UNCLASSIFIED
SECURITY CLASSIFICATION OF THIS PAGE (When Data Entered)

the digital method upgrades test reliability and performance and reduces operating cost by reducing total test time. These potential benefits made it attractive for the Harry Diamond Laboratories to undertake an effort concerned with the technical applications, and procedures related to the new test control method.

Test evaluation of the requirements for real-time digital computer control* of all pertinent test parameters indicates the new test method could be applied reliably to meet bare-table amplitude and frequency-control criteria of ±5.0 and ±0.2 percent respectively. These results were confirmed by data taken in the frequency range of 5 to 2000 Hz during both sine sweep and simulated resonance dwell operating modes. By contrast, present most restrictive requirements for conventional analog testing as specified in the test standards most widely used by the Army, i.e., MIL-STD-810B, -331 and -167 call for ±10.0-percent amplitude control and ±2.0-percent frequency control. It was further concluded that the computer-controlled-test technique could restrict amplitude quantization errors to ±0.5 percent if a 10-bit analog to digital converter is used in conditioning the test amplitude and that the equivalent analog amplitude distortions for the 128 points digitally synthesized sinusoidal waveform can be controlled to 0.5 percent over the frequency range of testing (5-2000 Hz). Furthermore, a dynamic range of at least 60.0 dB (typically required for most applications) is well within the capability of the new test method. Digital control testing has been incorporated into on-going qualification/acceptance testing of a variety of production weapon systems and components related to electronic fuzing.

Cost-effective measures that could reduce total test time by as much as one hour (or 25 percent for the typical mil-standard test) can be achieved when repeated (or variable mode) testing is required. This is accomplished through the utilization of preprogrammed and prechecked computer test tapes which practically eliminate the pretest setup and programming operations required in the conventional analog method. In addition, test reliability is significantly upgraded due to minimization of human errors. Therefore, a significant cost-effective measure can be realized if the new test technique is applied to large volume contractor or Army-wide production acceptance testing.

Substantial advancement relative to product quality control is another important derivative. Due to extended test capability digital control techniques could be used advantageously to test qualify production hardware to known service environments rather than to some "equivalent" test dictated by limitations of conventional analog testing. This subject however exceeds the scope of this report.

Also presented in this report are procedures for the implementation of direct-digital-computer control to Army sinusoidal vibration testing as well as the basic requirements for the applicable test equipment.

**Using Gilmore T5021 test system/C90 shaker.*

TABLE OF CONTENTS

Page

I GENERAL DESCRIPTION OF MTT PROGRAM EFFORTS BY HDL 11

1. INTRODUCTION 11

2. SUMMARY OF APPLICATIONS, IMPLEMENTATION, PROCEDURES, AND TECHNIQUES OF NEW TEST METHOD 12

2.1 Control and Performance Characteristics 12
2.2 Software Applications and Related Benefits 14
2.3 Tests to Establish Applicability of Concept 14
2.4 Control of Test Amplitude 15
2.5 Synthesis of Waveform 16
2.6 Digital Control During Simulated Resonance 16
2.7 Test Profile Repeatability 16
2.8 Real-Time Documentation and Summary 17
2.9 Test Programming and Elimination of Pretest Setup Operations 17
2.10 High Limits Vibration Tests Using Digital Control . 17
2.11 State-of-the-Art Test Techniques 18
2.12 Conclusions and Recommendations 18

II DESCRIPTION AND TECHNICAL OPERATIONS OF DDC SWEEP-SINE TEST METHODOLOGY, AND ITS APPLICATION TO ARMY VIBRATION TESTING PER MIL-STD-810B & -331 19

3. DIRECT-DIGITALLY CONTROLLED (DDC) SINUSOIDAL VIBRATION TEST SYSTEM 19

3.1 Gains Derived From Performing Military Tests on DDC Vibration Test Systems 19
3.2 Basic Sine-Control System 22
3.3 Basic Sine-System Software 23

4. SOFTWARE ORGANIZATION AND DESCRIPTION—SWEEP SINE TEST . 25

4.1 Program Procedure to Execute a Sine-Sweep Test . . . 25
4.2 Program Description 25

4.2.1 Bootstrap Program 25
4.2.2 Monitor Program 25
4.2.3 Editor/Compiler Program 26
4.2.4 Sine Operating Program 26
4.2.5 Data-Tape Program 26

4.3 Sine-Test Software Parameters Description—Basic Sine System 26

TABLE OF CONTENTS (CONT'D)

Page

4.3.1 Test Identification 26
4.3.2 Frequency Range 27
4.3.3 Transducer Sensitivity 27
4.3.4 Amplitude Profile 27
4.3.5 Test Duration (TD) 28
4.3.6 Compressor Speed 28
4.3.7 System Limits 29

4.4 System Flowcharts 30

5. MINIMUM SYSTEM HARDWARE 35

5.1 Feedback Signal Conditioning 35
5.2 Multiplexer and A/D Converter 36
5.3 Digital Processor (PDP-11) 36
5.4 Signal Synthesizer (D800) 37
5.5 Amplitude Control Precision Amplifier (D711) 37
5.6 Paper-Tape Reader/Teleprinter 38
5.7 Physical Environmental Requirements 38

6. ANALOG-TO-DIGITAL AND DIGITAL-TO-ANALOG CONVERTER 38

6.1 Technical Operations 38
6.2 Binary Number Representation and Quantization Error 40

7. DIGITALLY-CONTROLLED ELECTRODYNAMIC VIBRATION SYSTEM FOR SINE TESTING - TECHNICAL CONSIDERATIONS 42

7.1 Digital-Control Concept 42
7.2 Dynamic Range Considerations 43
7.3 Control Computer 43
7.4 State-of-the-Art Analog Test Equipment 44
7.5 Amplitude Control 46
7.6 Frequency Control 46
7.7 Sweep-Sine Digital Control System Configuration—Tracked/Untracked Modes 47

7.7.1 Overall Operations and Description 47
7.7.2 Untracked Mode 48
7.7.3 Tracked Mode 52

7.8 Generation of Shock Pulses and Shock Spectra 54
7.9 Computer Data for Digital Control of Sine Testing 55
7.10 Digital-Computer Word Format 56

TABLE OF CONTENTS (CONT'D)

Page

8. DIGITALLY-CONTROLLED SWEEP SERVO OSCILLATOR 58

8.1 Technical Considerations 58
8.2 Oscillator Considerations 59
8.3 Frequency-Synthesizer Section 61
8.4 Waveform-Synthesizer Section 63
8.5 Summary of Section 8 65

III TEST RESULTS, TEST DATA, HIGH-LEVEL TESTS, AND STATE-OF-THE-ART DEVELOPMENTS FOR DDC OF DYNAMIC TESTING 66

9. TESTS PERFORMED UNDER DIGITAL CONTROL 66

9.1 Vibration-Test Matrix 66
9.2 Test Fixture and Instrumentations 68
9.3 Data Acquisition System (DAS) 71
9.4 Instrumentation Description 73
9.5 DDC Test System—Electromechanical Limits 74

10. Test Data Analysis 77

10.1 Amplitude-Control Accuracy 77
10.2 Frequency-Control Accuracy 116
10.3 Strip-Chart Data, Computer Printouts, and Digital Synthesizer Waveform Data 118

10.3.1 Computer Printout 118
10.3.2 Analog Strip-Chart Data 119
10.3.3 Photographic Data of Digitally Synthesized Sinusoidal Input 155

10.4 Resonance Search and Dwell Tests and Data Obtained 155
10.5 Test Amplitude Repeatability and Voltage Drift Effects 162
10.6 Test Program Setup Time - Production/Qualification Testing 163
10.7 Summary of Acceptance Tests 164
10.8 State-of-the-Art Developments in Direct-Digital Control of Dynamic Testing 183

10.8.1 Manufacturers 183
10.8.2 Software Developments 183
10.8.3 Future Developments in Software Routines . 184

ACKNOWLEDGEMENT 185

TABLE OF CONTENTS (CONT'D)

Page

LITERATURE CITED 186

DISTRIBUTION 187

LIST OF ILLUSTRATIONS

Figure

1 Basic T5001 sine-control system—block diagram 22

2 Typical analog-to-digital and digital-to-analog conversion process 39

3 Acceleration to driving voltage ratio versus frequency . . 44

4 Block diagram for single-channel analog control test equipment 45

5 Block diagram of direct-digital control system hardware . 47

6 Block diagram for tracked and untracked digital control . 49

7 Sine wave synthesized from 128 clocked steps (32 polarity inverted steps) 59

8 Waveform synthesizer 60

9 Frequency synthesizer 61

10 Waveform synthesizer 64

11 Vibration test curves for cycling test for externally carried stores for helicopters 68

12 Vibration test fixture and instrumentation for DDC evaluation 69

13 Top view photograph of shaker, test fixture (circular plate); control accelerometer; monitor accelerometer; and two block mounted cross-talk accelerometers 70

14 Block diagram of data acquisition system (DAS) 72

15 Frequency calibration setup 74

16 Equivalent digitized amplitude voltage versus sweep frequency 90

17 Amplitude voltage plot for test No. 2 91

18 Amplitude voltage plot for test No. 3 92

19 Amplitude voltage plot for test No. 4 93

20 Amplitude voltage plot for test No. 5 94

21 Amplitude voltage plot for test No. 6 95

Figure	Title	Page
22	Amplitude voltage plot for test No. 7	96
23	Amplitude voltage plot for test No. 8	97
24	Amplitude voltage plot for test No. 9	98
25	Amplitude voltage plot for test No. 10	99
26	Amplitude voltage plot for test No. 11	100
27	Amplitude voltage plot for test No. 12	101
28	Amplitude voltage plot for test No. 13	102
29	Amplitude voltage plot for test No. 14	103
30	Amplitude voltage plot for test No. 15	104
31	Amplitude voltage plot for test No. 16	105
32	Amplitude voltage plot for test No. 17	106
33	Amplitude voltage plot for test No. 18	107
34	Amplitude voltage plot for test No. 20	108
35	Amplitude voltage plot for test No. 21	109
36	Amplitude voltage plot for test No. 22	110
37	Amplitude voltage plot for test No. 23	111
38	Total allowable error about test profile	113
39	Analog strip-chart data for test No. 3	145
40	Analog strip-chart data for test No. 4	147
41	Analog strip-chart data for test No. 9	149
42	Analog strip-chart data for test No. 17	151
43	Analog strip-chart data for test No. 18	153
44	Selected digitally synthesized sinusoidal input data for tests 15, 1, and 14	156
45	Selected digitally synthesized sinusoidal input data for tests 9, 8, and 16	157
46	Selected digitally synthesized sinusoidal input data for tests 6 and 7	158
47	Selected digitally synthesized sinusoidal input data for tests 13 and 4	159

LIST OF TABLES

Table	Title	Page
I	Amplitude and Frequency Control Requirements	15
II	Standard 10 Bits Conversion Code for Binary Numbers	41
III	Dynamic Range versus Format for Number Representation	58
IV	Test Matrix—Direct Digital Control of Army Sweep-Sine Vibration Tests	67
V	Average Sensitivity Factor for Test Accelerometers	71
VI	T5021 System/C90 Shaker Limits	77
VII	Test No. 1—Test Data Error Evaluation	79
VIII	Test No. 2—Test Data Error Evaluation	79
IX	Test No. 3—Test Data Error Evaluation	80
X	Test No. 4—Test Data Error Evaluation	80
XI	Test No. 5—Test Data Error Evaluation	81
XII	Test No. 6—Test Data Error Evaluation	81
XIII	Test No. 7—Test Data Error Evaluation	82
XIV	Test No. 8—Test Data Error Evaluation	82
XV	Test No. 9—Test Data Error Evaluation	83
XVI	Test No. 10—Test Data Error Evaluation	83
XVII	Test No. 11—Test Data Error Evaluation	84
XVIII	Test No. 12—Test Data Error Evaluation	84
XIX	Test No. 13—Test Data Error Evaluation	85
XX	Test No. 14—Test Data Error Evaluation	85
XXI	Test No. 15—Test Data Error Evaluation	86
XXII	Test No. 16—Test Data Error Evaluation	86
XXIII	Test No. 17—Test Data Error Evaluation	87
XXIV	Test No. 18,19—Test Data Error Evaluation	87
XXV	Test No. 20—Test Data Error Evaluation	88
XXVI	Test No. 21—Test Data Error Evaluation	88
XXVII	Test No. 22—Test Data Error Evaluation	89
XXVIII	Test No. 23—Test Data Error Evaluation	89
XXIX	Frequency Accuracy Data	117
XXX	Computer Printout of Test No. 3	120
XXXI	Computer Printout of Test No. 4	123

LIST OF TABLES (CONT'D)

Table	Title	Page
XXXII	Computer Printout of Test No. CPO-9	127
XXXIII	Computer Printout of Test No. CPO-17	130
XXXIV	Computer Printout of Test No. CPO-18	139
XXXV	Dwell Test No. 1	166
XXXVI	Dwell Test No. 2	167
XXXVII	Dwell Test No. 3	168
XXXVIII	Dwell Test No. 4	169
XXXIX	Dwell Test No. 6	170
XXXX	Dwell Test No. 7	171
XXXXI	Dwell Test No. 13	172
XXXXII	Dwell Test No. 14	173
XXXXIII	Dwell Test No. 15	174
XXXXIV	Dwell Test No. 16	175
XXXXV	Dwell Test No. 17	176
XXXXVI	Dwell Test No. 20	179
XXXXVII	Total Pretest Programming Setup Time	181
XXXXVIII	Limit Performance Sine Tests/T5021 System and C90 Exciter	182

I. GENERAL DESCRIPTION OF MTT PROGRAM EFFORTS BY HDL

1. INTRODUCTION

The Harry Diamond Laboratories (HDL) has recently applied and implemented a new test methodology sponsored by the Army Materials and Mechanics Research Center within the framework of the materials test technology (MTT) program. The work presented is concerned specifically with sine sweep and dwell testing, with primary emphasis on the Army's most widely used test standards for production/qualification vibration testing, MIL-STD-810B, transport (general purpose spec.) MIL-STD-331 (fuze/components specs), MIL-STD-167 (amphibious transport).

The method described employs a digital mini-computer with associated software and hardware peripherals that assumes direct and full control of sine-sweep and random vibration testing. Subsequent advancements have led to such direct computer-controlled options as shock-spectra testing, simulation of simple/complex acceleration-time transients, and automatic resonance search and dwell test techniques. The new digital-control system is designed as a replacement for the conventional analog test equipment because of increased reliability, accuracy, speed, and safety at reduced operating cost. The primary objective of this program is to upgrade current test requirements and procedures, as well as to apply the gains and cost-effectiveness associated with digital-computer control of dynamic testing to Army needs.

The concept of direct-digital-computer control of dynamic testing, along with associated electrical performance criteria, data processing routines, and software/hardware operation required to achieve real-time closed-loop control, has be considered in detail. It was concluded that direct-digital control of Army vibration testing is technically reliable, and that the new test method permits good compliance with all dynamic requirements imposed by the aforementioned specifications for the conventional analog test equipment. An extensive test program was subsequently initiated to establish the validity of this conclusion. Representative tests from MIL-STD-810B, -331 and -167 were performed under direct computer control simulating maximum/nominal/minimum Army field environments. Analysis of the test data strongly confirmed this conclusion. The required ±10-percent amplitude control accuracy and ±2-percent frequency control accuracy in the 5- to 2000-Hz band were adequately met by the new test system which demonstrated amplitude and frequency perturbations of about 5 ± 1 percent and under 0.2 percent,* respectively, during cycling and simulated resonance dwell operations. Also demonstrated under direct-digital control were vibration-test parameters far in excess of those listed in these specifications, with almost comparable control accuracy (i.e., sustained 120 g levels at sweep rates of 0.1 to 7.0 octaves/min within the 5- to 3000-Hz band).

**Except at 10 Hz where frequency error was ±0.5 percent.*

The implementation also revealed that the new test method could bring about a substantial cost reduction of approximately 25 percent to Army-wide vibration testing of the tests specified herein.† This approximation was based on the fact that a computer-controlled test system using permanent storage of preprogrammed test tapes eliminates the need for the (approximately) 1-hr setup time typically required in programming conventional analog test equipment. Consequently, maximum duration tests specified in MIL-STD-810B could be reduced from an average 4 to 3 hr; substatntially larger cost reductions can be expected for the shorter duration tests. Owing to the numerous benefits derived from digital control testing, the new test method has been incorporated into HDL on-going qualification/acceptance testing of production configuration missile and artillery electronic fuze systems and components. Among the systems/components already tested were the XM817/818 missile fuzes, XM587 and XM728 artillery fuzes, and numerous other production hardware.

Section 2.1 below describes design performance, operations, control and dynamic range capability of the new test system vis-a-vis the specifications invoked requirements. Section 2.2 qualitatively outlines software applications and potential benefits associated with the new test method (refer to Ch III for details of sections 2.1 and 2.2). Sections 2.3 through 2.9 contain quantitative results indicating that the new test method can be applied reliably to perform the type of vibration tests listed in the aforementioned specifications. Section 2.10 contains test data to the effect that the new test technique can also be used to execute high-level vibration testing. Section 2.11 summarizes those advances in the state-of-the-art that could be advantageously incorporated into Army-wide shock and vibration testing.

The technical effort and subsequent testing were performed using the Gilmore/MB Electronics T5021 Digitally Controlled Vibration Test System/C90 Shaker currently in operation at this facility. Fundamentally, all direct digitally controlled test systems are designed around the same closed-loop control concept.

Future plans include applications, techniques, and procedures relative to the utilization of digital computer control to the Army's production/qualification random vibration testing and shock testing requirements.

2. SUMMARY OF APPLICATIONS, IMPLEMENTATION, PROCEDURES, AND TECHNIQUES OF NEW TEST METHOD

2.1 Control and Performance Characteristics

The concept and requirements associated with real-time computer control of vibration testing have been evaluated and analyzed in detail. Specifically considered (and discussed in detail in Ch II of this report) were the following items (a) through (j):

(a) closed-loop signal-control logic,

†*Except for long duration transportation vibrations.*

(b) control-signal analog to digital-conversion technique and the resulting quantization error,

(c) computer data sample rate,

(d) excitation signal filtered/unfiltered digital processing and control criteria,

(e) amplitude and frequency control accuracy and limits violation thereof leading to ABORT/ALARM status,

(f) signal forward/feedback precision gain and scaling conditioning circuitry,

(g) digital synthesis of harmonic drive signal using sweep-servo oscillator,

(h) software organization and test program preparation,

(i) test-data documentation, and

(j) test reliability and total setup time for repeated production/qualification testing.

The characteristics of the digitally-controlled forward-precision-gain amplifier and feedback-scaling amplifier required for conditioning the vibrations control signal indicate a dynamic range capability of at least 60 dB and a gain accuracy of 1 percent of full-scale output for this test control technique. Quantization errors associated with the 10-bit analog-to-digital converter (of the vibration signal) were about ±0.5 percent.

The digital oscillator was configured to yield an equivalent analog waveform distortion level of less than 0.5 percent and fine frequency programming control accuracy of 0.1 percent of point in the 0.5- to upward of 10-kHz band. The oscillator digitally synthesizes a harmonic cycle from 32 voltage steps polarity-inverted quarter-cycle sine wave, generating a total of 128 points. The fine frequency resolution in any octave is obtained by dividing the frequency in steps of 2^{10}, which is accomplished through the implementation of digitally controlled phase lock loop, a precision-controlled clock oscillator that prevents frequency drift for whatever reason. Software and hardware implemented filtering technique permits the computer to interpret and control the test amplitude to a wide band or selectively tracked frequency. Data sample rate, typically maintained at 512 samples/sec above 12 Hz, is adequate in maintaining package safely, as the maximum (number of consecutive) data frames required to abort (32 frames) will result in out-of-bound test time of 0.0625 sec (except as modified by system's inertia; below 12 Hz, this time could increase to 0.125 sec).

A comparison between three of the most used methods for computer arithmetic (to represent the test data) i.e., fixed point, floating point, and logarithmic, indicates the floating point (scientific) notation to be the most efficient for sine-sweep testing and best adaptable to the 16-bit mini-digital computer, providing high-speed data processing algorithms are used.

In view of the technical performance of the system, it becomes apparent that direct-digital-computer control of Army vibration testing is technically attainable and reliable, in fact most desirable due to its advantages over the conventional analog technique, and that the ±10-percent amplitude control accuracy and the ±2-percent frequency control accuracy requirements (specified in most current standards for analog testing) are well within the capabilities of this test-control method.

2.2 Software Applications and Related Benefits

Efficient software organization, straightforward test programming, and simplicity of operation can be accomplished with test process oriented digital mini-computers. To program a test, all that is required is an editing routine in conversational language. Operator-supplied test information is computer checked and then punched on an 8-bit paper tape or other input devices used to commence testing. Once the programmed tape has been fed into the computer, the entire test sequence—including real-time monitoring, documentation, and shutdown—proceeds automatically under computer control. The primary benefits that can be derived through the application of direct-computer control to dynamic testing are summarized as follows:

- Practical elimination of pretest setup operation through the use of preprogrammed tapes—a particularly attractive feature for large-scale production testing. By contrast, analog test equipment requires on-line programming or/and adjustments for every test.
- Substantial improvement in reliability as human interference, and therefore human error, is kept to a minimum.
- Instant post-test complete documentation and analysis of test data (also not available with analog testing).
- Safe operation as each test parameter is (continuously) computer checked. No special programming skills required as programming is implemented in conversational language.
- System is designed around building block concept permitting quick expansion to other forms of testing through peripherals or standard tape program library.

2.3 Tests to Establish Applicability of Concept

An extensive test series was initiated to confirm the application and compliance of direct-digital-computer control to Army vibration

testing requirements. Twenty-three tests were selected from test standards most commonly used by the Army for production/qualification testing of the applicable weapon systems (MIL-STD-810B, -331, -167, and the newly proposed MIL-STD-810C), extending over the entire spectrum of field environments. An analysis of the data from all tests indicates excellent compliance with the specifications-invoked accuracy-control requirements for amplitudes and frequencies. The test results are summarized in table I below.

TABLE I. AMPLITUDE AND FREQUENCY CONTROL REQUIREMENTS

Specification Requirements		Test Results*
Amplitude Control:	±10% of specified value†	5 ± 1%**
Frequency Control:	±2% of specified value***	±.1% (maximum) at 5 Hz ±.5% (maximum) at 10 Hz
	20 Hz	under ±.2% 20-2000 Hz
	+1/2 Hz below	±0.05 Hz below 20 Hz
Frequency band:	5-2000 Hz	5-2000 Hz

*Refer to sections 9.2 and 9.3 for description of test instrumentation and fixture.
†Plus or minus 20 percent for MIL-STD-167
**Average amplitude error was centered at about 5 percent about the specified value, with a ±1-percent band fluctuation. Refer to sections 10.1 and 10.2 for data-error analysis.
***Plus or minus 3 percent for MIL-STD-331

Extraneous system noise, evidenced in the early stage of testing, resulted in amplitude control in excess of the allowable ±10-percent band when operating at low frequency (5-15 Hz) and low displacement (0.1 in. D. A.). This was due to the fact that at low frequency, the equivalent acceleration level could be as low as 0.15 g, for which the control transducer output voltage (appx. 40 mV/g) fell below 10 mV (i.e., within the noise region). To remedy this, the signal-to-noise ratio was increased approximately by 2.5:1 (to 100 mV-Pk/g) through the incorporation of an additional scaling/charge amplifier in the feedback loop. Amplitude control was then reestablished within the ±10 percent band.

NOTE: The digital real-time control capability of the test system method was further substantiated by its ability to compress resonance buildup to within ±10 percent. Test data at 2000 Hz indicate the (C90-shaker) bare table axial resonance to be approximately 4:1. However, data included herein (for the instrumented shaker) show the test amplitude was controlled to 7 ± 1 percent of the specified value at 2000 Hz, both in the sweep mode as well as during a 30-min dwell operation.

2.4 Control Techniques for Test Amplitude

Amplitude control can be achieved for digital tracked/untracked operations. Under untracked operation, the magnitude of the feedback signal (used as basis for control) may consist of frequency components

made up of the fundamental frequency as well as of contributions from harmonics and noise. This assures excitation to a desired amplitude but not necessarily at the specified frequency (i.e., the fundamental amplitude at a specific frequency may be significantly lower than that required). However, when the control system is programmed for tracked operation, the feedback signal is digitally processed and controlled to the fundamental amplitude at the absolute sweep frequency only. Amplitude control is therefore assured at the specified frequency (refer to section 7.7 for detailed discussion).

2.5 Synthesis of Waveform

Photographic data indicate the digital oscillator can synthesize a smooth harmonic drive signal from a 32-step polarity-inverted quarter cycle sine wave. The average combined* distortion, measured at the center of the fully powered bare exciter, was below 1 percent in the 5- to 2000-Hz band.

2.6 Digital Control During Simulated Resonance

Extensive simulation of resonance dwell testing was performed under direct-digital control. Resonance frequencies were specified within the 5- to 2000-Hz band and for dwell periods in accordance with the specifications requirements. A significant number of the (simulated) resonance frequencies was selected at regions for which direct-computer control might be particularly difficult to implement, such as dwells at points (5 or 2000 Hz), acceleration/displacement crossover frequency(s).

The prime objective, direct computer control of the specified amplitude level(s) for 20 to 30 min of continuous dwell operation, was successfully demonstrated. No frequency drifts or out-of-bound amplitude deviations were noted in the dwell periods. Shaker axial resonance buildup at 2000 Hz (with fixture/instruments) was continuously compressed to within the required ±10-percent control during a dwell period lasting 30 min.

Present resonance dwell operations on this system require the operator to manually abort the sweep test and command the system to dwell at a test frequency which is also determined manually. The dwell operations are automatic from that point and insure that any out-of-bound perturbations will cause system abort. To terminate dwell, a manual shutdown command is required. Recent software developments, however, permit the execution of this entire operation automatically for an operator-defined-resonance level and dwell time, provided at least two computer data channels are available for transducers relative measurements. However, if control at a known resonance frequency and location is desired, a single transducer is required.

**Combined characteristic electrical and mechanical distortion of shaker.*

2.7 Test Profile Repeatability

Review of analog strip-chart data for all tests (these data records are not a part of the digital-control system but were used for monitoring purposes) indicates excellent repeatability of the programmed test profile over as many sweep cycles as specified. The specification-imposed amplitude and frequency-control requirements were maintained throughout the cycling.

2.8 Real-Time Test Documentation and Summary

Real-time documentation is available in the form of hard-copy digital listing of the specified vis-a-vis the executed test profile at every 1/3 octave point (optional listing can be affected at any frequency). The computed value of the executed test mode is based on any desired statistical average of the test amplitude (in this case an arithmetic average collected over 0.5 to 2.0 sec prior to the listed test time; the data window is optimized with sweep speed and test frequency). In-between points are monitored by the computer but not listed. A backup data source is the x-y plot of the digitized peak amplitude voltage (or amplitude rms voltage) versus frequency. Together, these data form an acceptable and coherent record of the test, and are instantly available at the completion of the test for test evaluation. The relatively slow ASR-33 teletype supplied with this system will skip listing for sweep speeds in excess of 3.0 octaves/min. However, all tests performed herein are limited to sweep speed of approximately 1.0 octaves/min, and standard military testing is not performed above 3.0 octaves/min.

2.9 Test Programming and Elimination of Pretest Setup Operations

Based on this test system tape read/punch/type equipment (see sect 5), the average total programming time for tests performed herein was 17.75 min with no advanced preparations whatsoever (i.e., "cold start"). Once all the necessary tapes have been programmed, the total setup time required to initiate testing decreased to 4.15 min, a time saving of about 77 percent compared with cold start. The practical elimination of the setup time can be achieved by storing all test program and data tapes on a disc system, and recalling the desired test directly into the computer. It is estimated that due to the high-loading rate of the computer (PDP-11/20), this procedure will require only a fraction of a minute, representing upward of 76-percent improvement over method of input of preprogrammed 8-bit paper tapes and upward of 95-percent improvement when compared with the cold start. By contrast, the equivalent setup time associated with analog test equipment could typically be on the order of 1 hr. As the longest test specified in MIL-STD-810B lasts approximately 3 hr, the total test time could be reduced from 4 to 3 hr through the elimination of the setup time.* A significant cost reduction of about 25 percent per test could be realized here, a particularly attractive cost-effective measure when applied to *all* Army and contractor vibration testing. (Refer to section 10.6 for test-time data. Indicated times do not account for fixture installation.)

**The 4-hr figure contains 1 hr of setup time associated with analog test equipment.*

2.10 High Limits Vibration Tests Using Digital Control

Vibration levels far in excess of those specified in MIL-STD-810B and MIL-STD-331 were successfully executed under direct-digital-computer control. These included:

(a) A 10-level acceleration velocity displacement test profile between 5 and 3000 Hz, at sweep speeds of 0.1 to 7.0 octaves/min, and maximum systems limits which are: 120-g acceleration, 50-in./sec velocity, and 0.75-in. (D.A.) displacement.

(b) Sustained acceleration levels of 120 g, 50 in./sec velocity, 0.75-in. D. A. displacement accompanied by 60-dB steps with a total payload of 12 lb. System abort limit was set at ±1.0 dB.

2.11 State-of-the-Art Test Techniques

Current state-of-the-art software developments indicate that the following direct-computer-controlled test operations are potentially adaptable to standard and/or special Army vibration-shock testing:

(a) Random and mixed sine/random with automatic compensation for shaker/load dynamics, and quick equalization time.

(b) Multichannel and multishaker amplitude/phase control capability.

(c) Shock-spectra synthesis accompanied by automatic compensation for shaker/load at specified levels of error and damping.

(d) Simulation of most field shock environments through the electronic synthesis of simple/complex acceleration time histories.

(e) Automatic resonance search/dwell routine permitting execution of sine-sweep resonance search, dwell, and shutdown operations with no human intervention.

2.12 Conclusions and Recommendations

(a) Technical considerations supported by extensive application testing demonstrated that the direct-computer-controlled test methodology complies with the Army's needs and specifications governing sine-sweep vibration testing. The numerous benefits offered, particularly in the area of cost effectiveness and improved test reliability/performance, make the new test method most desirable for the Army's production/qualification vibration testing. HDL has implemented the new test method in the qualification/acceptance testing of a variety of production and pre-production weapon systems and components related to missile and artillery electronic fuzing.

It is therefore recommended that the direct-computer-controlled test method be incorporated into all Army sine-sweep vibration testing, without the need to compromise the outstanding specifications. It is

further recommended that the existing specifications (particularly some of the most commonly used by the Army such as MIL-STD-810B, -331, and -167) be updated in light of the more realistic simulation capabilities offered by this test technique, and presented in this report, to affect vibration testing under a wider range of dynamic environments and tolerance limits not currently practical with conventional analog equipment (i.e., increase the total number of mixed mode test steps; restrict amplitude control errors, etc.)

(b) Continue the technical and test effort under the MTT program, to establish the adaptability, benefits, cost-effectiveness, and applications testing of the state-of-the-art developments defined in section 2.11, vis-a-vis the on-going shock and vibration testing requirement for Army materiel.

II. DESCRIPTION AND TECHNICAL OPERATIONS OF DDC SWEEP-SINE TEST METHODOLOGY, AND ITS APPLICATION TO ARMY VIBRATION TESTING PER MIL-STD-810B & -331 & -167

3. DIRECT-DIGITALLY CONTROLLED SINUSOIDAL VIBRATIONS TEST SYSTEM

HDL operates a DDC vibrations test system for the purpose of performing acceptance and/or qualification testing of production weapon systems per the specified military standard (most commonly MIL-STD-810B, -331, -167) or other special testing requirements. The (T5021) DDC test control system, manufactured by Gilmore Industries, consists of the basic (T5001) sine operating system, the basic (T5020) random operating system, and the mixed mode sine/random option. These test control capabilities are further supported by Fourier/PSD analysis techniques to evaluate the characteristics of the test drive/feedback signal. This report is restricted to procedures, techniques, and application testing relative to the sinusoidal vibrations test method--supported by extensive test data. The foregoing results, although derived from the use of the specified test equipment, can be considered representative of the DDC test technology. Fundamentally, all DDC test systems operate around the same close-loop real time dynamic control concept.

3.1 Gains Derived From Performing Military Tests on DDC Vibration Test Systems

This section summarizes the numerous benefits offered by the new DDC vibration test method over the present day analog test technique. The particular adaptability of the DDC test technique to sine testing per Military Standards becomes quite apparent.

Computer control of vibration production, qualification, or simulation tests promises substantial operating-cost reduction previously not attainable. This is due primarily to the marked reduction in pretest setup time and reduced number of skilled operators required to execute these tests (in fact no programming knowledge is required to operate the system). Additional cost savings are incurred when preprogrammed test tapes are used again and again in test operations, thereby practically eliminating test setup time. Test reliability is also enhanced because human errors are eliminated through computer control. The classical slip of "forgotten switch," or control adjustment, no longer exists for tests of the highest complexity. The test tapes may also be permanently stored on a disc system and called directly into the computer; thus, additional time-saving is realized due to the elimination of the tape-reading sequence.

Complete control over the system is possible during the test. The operator can stop, start, change test profile or dwell at any point in the test through a manual override password communicated to the computer via the teletype. For extremely accurate sine tests, automatic amplitude control can be maintained to levels as low as ±0.5 dB (approx ±6 percent), whereas typical military sine-vibration tests require control accuracy of ±10 percent (approx ±0.9 dB). Operating cost is further reduced as the system also provides complete test documentation. Each test profile is fully documented in real time, yielding amplitude levels, frequency range, sweep rate, control limits, and test-time information. At the completion of the test, an instant test history that is free of human error is provided. In the manual operating mode, the operator has the option of setting the test to 1/4 and 1/2 levels prior to proceeding at full level in the automatic mode.

The DDC vibration system is built around a flexible building block concept. The basic sine system can be expanded to include complete sine-shock, random, and mixed sine/random test capability; also, it can be used for real time-data analysis. These capabilities are achieved by adding the appropriate peripheral hardware components and the corresponding software routines. When no tests are performed, the 4th generation 16-bit (8092-word memory) computer may be used for direct programming and computations in basic language.

The versatility of the DDC system is further enhanced by its ability to produce simple or complex SHOCK pulses at the shaker head by direct programming, thereby permitting the simulation of shock-spectra environments. The exciter, in effect, becomes a versatile shock/vibration apparatus. The setup time for pulse shaping is eliminated as each pulse is shaped electrically, and the load/shaker transfer function is automatically accounted for in the program.

Present day DDC vibration systems offer up to 8 channels of data-processing capabilities and control. Test amplitude control can be based on any standard averaging techniques, or the system can be used to control several shakers simultaneously. The primary benefits offered by a DDC vibration system over the conventional analog equipment can be summarized as follows:

Reduced Operating Cost*

- Reduced test setup time
- Human error practically eliminated
- On-line/off-line data analysis
- Complete test documentation
- Improved reliability

Safety

- Test parameter computer checked
- Automatic shutdown if allowable limits are exceeded
- Alarm messages when allowable limits are intermittently exceeded

Simplicity

- Question/answer routine in conversational english during programming
- No special programming skills required
- Completely automatic operation
- Standard test tape library available
- Abort/test preparation diagnostic message listing
- Preprogrammed test tapes available on disc

Flexibiltiy & Versatility

- Building block capability
- Sine/random/mixed sine-random/analysis/shock capability
- Multiple channel control (up to 8 channels)
- Real time/off-line fast fourier transform analysis and PSD analysis
- General purpose computer analysis during off-test period
- Multishaker control

**Refer to section 10.6 for data on total setup time.*

3.2 Basic Sine-Control System*

A functional block diagram of the Gilmore Ind. basic sine-control system is presented in figure 1. The main feature of the system is its use of a small digital computer in direct, closed loop, control of the forward and feedback signals. Peripherals controlling and monitoring such parameters as loop gain, test profile, and frequency are constantly under direct-digital control. The system is capable of accepting up to 10 program levels in any combination of acceleration, velocity, or displacement at sweep speeds ranging between 0.1 and 7.0 octaves/min in the frequency band of 5 to 3000 Hz.

Fundamentally, the operation of the system is based on the computer-controlled D701 zero drive amplifier that provides the necessary signal conditioning for the feedback signal. The D710 amplifier provides precise incremental gain control to normalize the feedback signal. Conditioned output from the D710 module is processed by the D726 unit where rms level proportional to amplitude is generated for the feedback signal. The output of the D726 is then sampled by the variable rate analog-to-digital converter, and is coded into binary numbers representing amplitude information. The binary numbers are then communicated to the PDP11 computer through the D706 interface (buffer) module. The PDP11 computer inputs these numbers (test data) into a software routine that compares the test level to the desired profile.** If any inconsistencies between these levels develop, the computer will automatically adjust the forward path gain controlled by the D711 precision amplifier, and will set the optimum servo response time as a function of sweep rate. Waveform synthesis and test

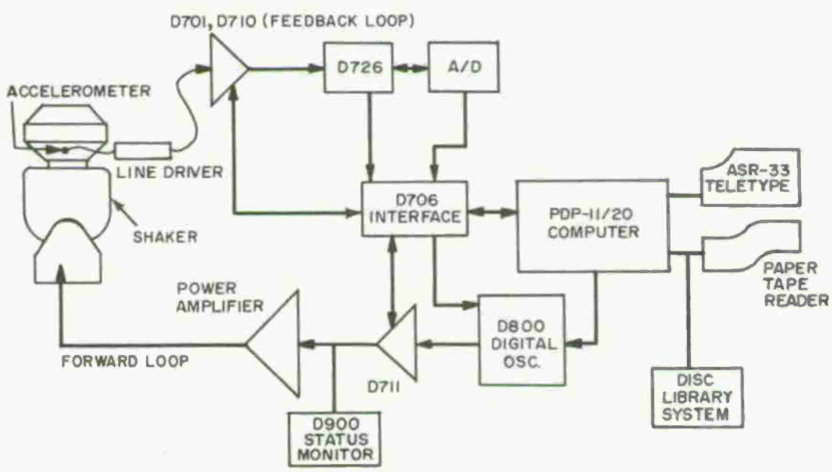


Figure 1. Basic T5001 sine-control system—block diagram.

*Refer to section 7 for detailed description and operation.

***The desired test profile has already been furnished to the computer during the setup routine.*

frequency are generated by the D800 computer-controlled digital oscillator. Communications between the PDP11 computer and the digital oscillator are internal and are based on binary language. Closed-loop direct digital control is thus maintained throughout the test envelope.

3.3 Basic Sine-System Software

This is a setup and editing routine that permits the operator to program a multi-level sine test (up to 10 levels of acceleration, velocity, or displacement within the frequency range of the equipment), through a question and answer series in conversational language. No programming skills are required. Each test entry is checked against the maximum permissible limits which are permanently stored in the computer. The operator is required to define the allowable deviations from the specified profile, beyond which the test will be automatically terminated. After the test definition has been completed, a paper (data) tape is generated. Also generated is a hard copy from the teleprinter listing all test parameters. The sine operating tape is then fed into the computer followed by the data tape to initiate the test. A real-time override of specific test parameters is also possible through the use of a special password. During the test the teleprinter will list the actual-versus-desired test mode as a function of test time at each 1/3 octave points as well as all profile crossover frequencies. Another test-data source available is a plot of the feedback digital voltage as a function of frequency. This voltage can be used to ascertain accelerometer output in between the 1/3 octave points (however, it is not quite an analog signal). A more detailed discussion of the software package is presented in the section on software organization. Listed below are the T5021 DDC system hardware/software components.

Hardware Components

PDP-11	Mini-computer - S*, R**
RK-11/02	Disc Memory System - S, R
ASR-33	Teleprinter - S, R
Varian 620	Mini-computer (FFT-BOX) - R
HP-1205B	Oscilloscope - S, R
D820	Paper Tape Reader/Puncher - S, R
N166-3	X-Y Recorder - S, R
D706	Computer-Process Interface - S, R
D705	Computer-Computer Interface - R

*Sine test
**Random test

Hardware Components (Cont'd)

D900	Safety Status Register - S, R
D811	Multiplexer and Analog/Digital Converter - S
D800	Function Generator - S
2 D701/710	Feedback Path Amplifiers - S, R
2 D711's	Forward Path Amplifiers - S, R
D730	Dual Digital/Analog Converter - R
D720	Shock System Signal Conditioner - S
2 D726	Sine System Feedback Signal Processor - S
2 D735	Random System Signal Conditioner - R
D736	Random Number Generator - R
D720X	Filter - S
C-90 & Power Amplifier	Shaker System - S, R

Software Components

Monitor 5B (In permanent residence)

Sine Editor/Compiler - S Sine-Shock Editor/Compiler - S Random Editor/Compiler - R Sine/Random Editor Compiler	Required to prepare test (data) tapes
Sine Operating System - S Sine-Shock Operating System - S Random Operating System - R	Required to execute test

Analysis Operating System (Editor/Compiler on same tape

-S, R (for off-line data)

4. SOFTWARE ORGANIZATION AND DESCRIPTION—SWEEP SINE TEST

This section summarizes all program routines and procedures necessary to perform a sine-sweep test.

4.1 Program Procedure to Execute a Sine-Sweep Test

The following program tapes, in the order shown, must be loaded into the computer to execute a sine-sweep test:

(1) Bootstrap program

(2) Monitor program

(3) Sine operating program

(4) Data tape program

To prepare a data tape program, only tapes (1) and (2) must be loaded. An editor/compiler tape program is then entered, and a data tape is edited according to the desired test profile. The editor/compiler is then used to punch out a binary (8 bits) paper tape containing the entire test information; this is the required data-tape program (4).

The editor/compiler program is erased from memory prior to testing according to a procedure described below. All programs, except for the data tape, are supplied with the system. All that is required is to load them in.

4.2 Program Description

4.2.1 Bootstrap Program

The bootstrap program is the routine that reads in the monitor program. It is required to initiate the computer, and is made necessary due to the fact that the computer cannot read in any program unless it is executing reading instructions (i.e., the computer lacks reading instruction to execute readings). For this reason the bootstrap program is fed in through a series of control panel switches. It is the only program not stored on tape.

In this routine only 10 binary numbers are quickly loaded into the computer. This program is loaded in very infrequently as the monitor program is usually always in residence.

4.2.2 Monitor Program

This program resides in memory and is required to load into memory either the editor/compiler program or the sine operating system. It also contains computer instructions related to various electronic housekeeping instructions needed by the teleprinter and paper reader.

4.2.3 Editor/Compiler Program

This program translates into machine language a series of questions and answers used to prepare the data tape. Hence, to prepare a data tape the editor/compiler program must already be loaded. Since the editor/compiler program practically consumes the bulk of the memory, no core is available for computer instructions to carry out the test. This necessitates the creation of a separate data tape which contains the entire test information.

Initially, the program presents a set of questions that must be answered to describe the test. The machine asks the questions and the operator supplies numerical or conversational answers on the teleprinter. The operator is permitted to erase old entries and substitute them for new ones. A final, updated listing of all test entries is then printed out. This information is the hard-copy documentation, and is later coded in binary language on a data tape. The editor/compiler program also checks each test entry against the maximum permissible limits specified for that test parameter.

4.2.4 Sine Operating Program

The purpose of this program is to inform the computer that a sine test is requested. The program, in effect, carries out the test and prepares the memory to read in the data tape. When loading in the sine-operating program, the editor/compiler program is automatically erased from memory.

4.2.5 Data-Tape Program

This tape contains all test information related to amplitudes, frequencies, sweep rate, time abort limits, and mode profile, all binary coded. The computer will automatically control the test according to the information supplied by this tape. The tape can be used again and again to repeat the test. However, new data tapes must be edited if any changes in the punched test are required. Approximately 1 min is typically required to read a 10-level program tape into computer memory.

4.3 Sine-Test Software Parameters Description—Basic Sine System

The foregoing discussion is related to the software package of the basic T5001 sine-sweep system. Generally, all digitally controlled sine-sweep test systems are subjected to similar consideration and restrictions imposed on their software routines.

4.3.1 Test Identification

A free field block permits the operator to enter identifying information up to 72 characters in length. This identification section consists of five lines in which data must be entered for each line or an error will occur. The identification section will be punched on the beginning of the data tape to provide fast identification of the tape.

4.3.2 Frequency Range

The sweep sine testing may be defined over any continuous range between 0.5 and 16.0 kHz.* The operator is requested to specify the following frequency parameters:

(1) Lowest test frequency

(2) Highest test frequency

(3) Sweep starting frequency

(4) Initial sweep direction

These entries are tested against the minimum and maximum permitted frequencies. The system sweep is logarithmic in both up-sweep and down-sweep modes. The digital system is capable of specifying frequency to 0.1 percent of point.

4.3.3 Transducer Sensitivity

The operator is able to specify accelerometer sensitivities in both millivolts/g and picocoulombs/g, depending on whether voltage or charge sensitive line drivers are used. The system can accommodate sensitivities in the range of 1 to 10,000 mV/g.

4.3.4 Amplitude Profile

The system permits the operator to specify amplitude profiles with up to ten levels.

The test levels are specified directly in terms of displacement (inches pk-pk), velocity (in./sec), and acceleration (g units). These are entered as:

D - Displacement

A - Acceleration

V - Velocity

Any letter other than A, V, or D will cause an error to occur. The system is capable of automatically computing the crossover frequency between amplitude parameters of displacement, velocity, and acceleration.

The system automatically checks the operator-entered amplitudes to insure that they are within predefined** maximum and minimum limits. If the limits are exceeded, the system will print appropriate error codes and prohibit running of the test.

*Actual frequency range is restricted to shaker/amplifier limitations.
**Test equipment limitations.

The system permits the operator to specify two tolerance levels for each amplitude level. The first tolerance level is an alarm point specified in ±dB. The system will alarm by printing appropriate frequency and amplitude information on the test recording paper. The second tolerance level is an abort level, in ±dB, which is equal to or greater than the alarm level. The system will initiate a controlled shutdown if this tolerance is exceeded. In addition, the system will print appropriate data on the teleprinter.*

The system permits specification of tolerances from ±0.5 to ±50.0 dB. The system will monitor the control signal and initiate appropriate alarm or abort action for any out-of-tolerance condition, including conditions caused by loss of feedback signal. Loss of feedback signal may be any failure of the transducer mount, or signal line including failure to connect the signal line.

4.3.5 Test Duration (TD)

The system permits the operator to define two of three parameters for test duration. The parameters are:

(1) Time in minutes,

(2) Sweep cycles, and

(3) Sweep speed in octave/min.

The operator has the option to select the two parameters. Time is specified in minutes or decimal parts of a minute. Sweep cycle is defined as two reversals in sweep direction (i.e., from lowest frequency to highest frequency and back to lowest frequency). The system accepts numbers equal to integer sweep cycles (i.e., sweep from lowest to highest frequency), and will accept sweep speeds from 0.1 to 7 octaves/min. The system computes the unspecified parameter from the two operator-entered parameters. A listing is automatically forced before punching; therefore, all data punched are correct. Faulty data can never enter the system. Any inconsistency in data causes an appropriate error message to be printed and prohibits system operation.

4.3.6 Compressor Speed

The servo compressor speed is automatically optimized by the digital processor and has a range of 0.5 dB/sec to 2000 dB/sec. The servo control routine is capable of compressing:

(1) Errors in the control loop to virtually zero error within the dynamic range of the system.

**Abort can be initiated based on any desired number of successive out-of-bound data frames. The levels causing ABORT will be printed out.*

(2) Error signals not compressed to zero, and outside the operator-specified tolerance levels, cause the system to take appropriate alarm or shutdown action.

(3) The fastest system's speed control requires a Q of 50 or less. The operator can counteract expected load resonances by choosing specimen Q of L, M, or H.

High Q	$Q > 200$
Medium Q	$50 \leq Q \leq 200$
Low Q	$0 \leq Q \leq 50$

4.3.7 System Limits*

The system permits test-parameter limits to be entered via the teleprinter keyboard. This capability is protected, so that operating personnel cannot alter the limits without authorization. All limits are entered in the same test engineering units as used for test definition.

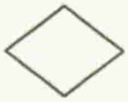
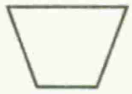
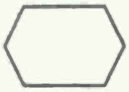
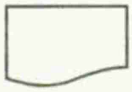
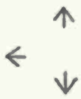
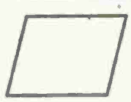
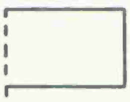
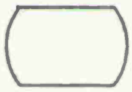
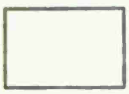
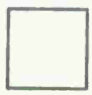
The system permits entry of maximum and minimum limits for the following parameters:

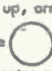
(1)	Frequency	(0.5-16000.0) - Hz
(2)	Displacement	$(1 \times 10^{-6} - 20)$ - in. D. A.
(3)	Velocity	$(1 \times 10^{-3} - 100)$ - in./sec
(4)	Acceleration	(0.05 - 300) - g
(5)	Accelerometer sensitivity	(1.0 - 1000.0) - mV/g
(6)	Alarm/abort	(0.5 - 50.0) - dB

**System limits presented here reflect the electrical limitations of the control hardware. Actual system performance is dictated by the power amplifier/exciter limitations.*

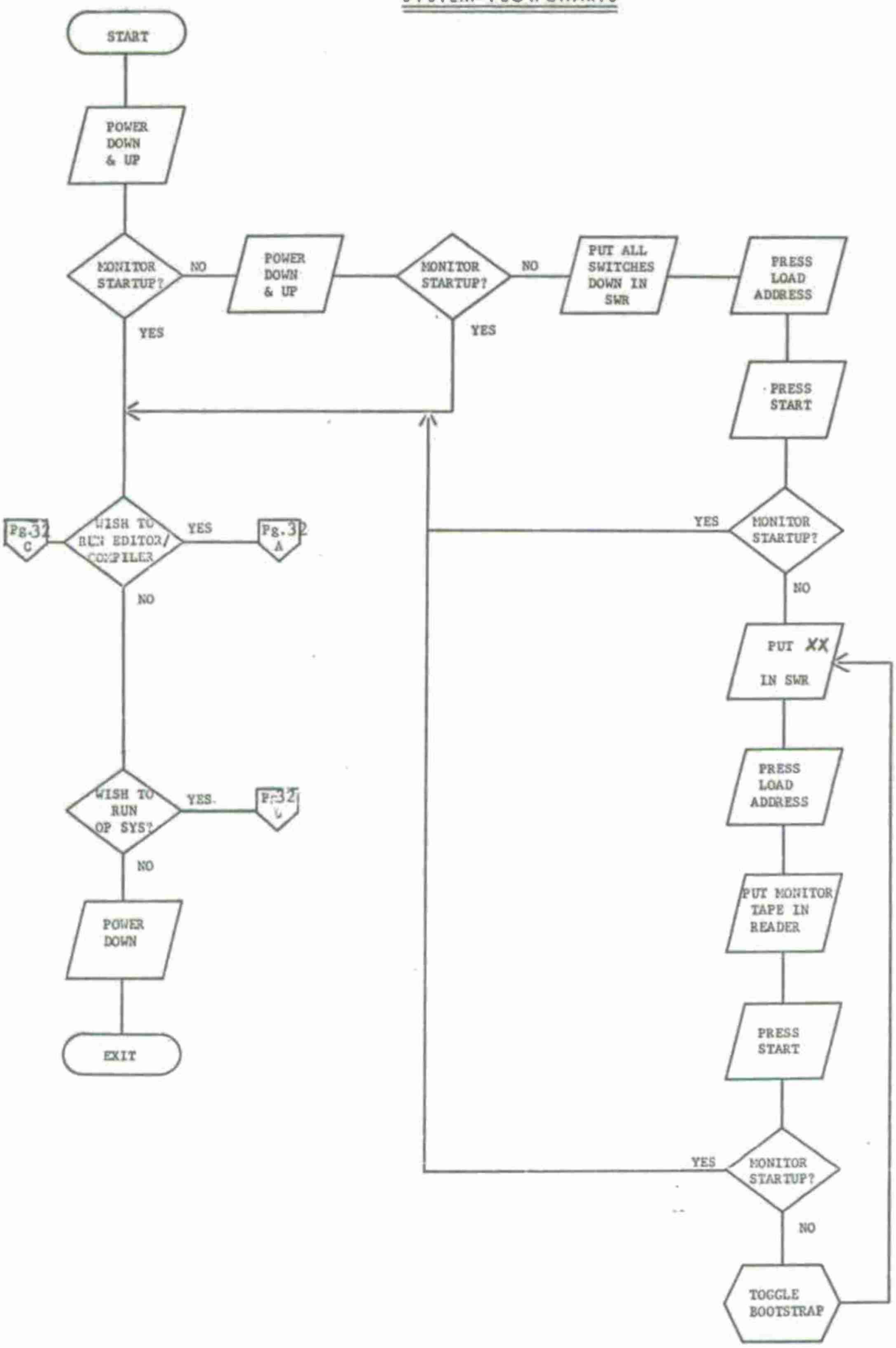
4.4 System Flowcharts

The flowcharts included give a pictorial representation of the system operation. Each block represents a particular function in the system, such as:

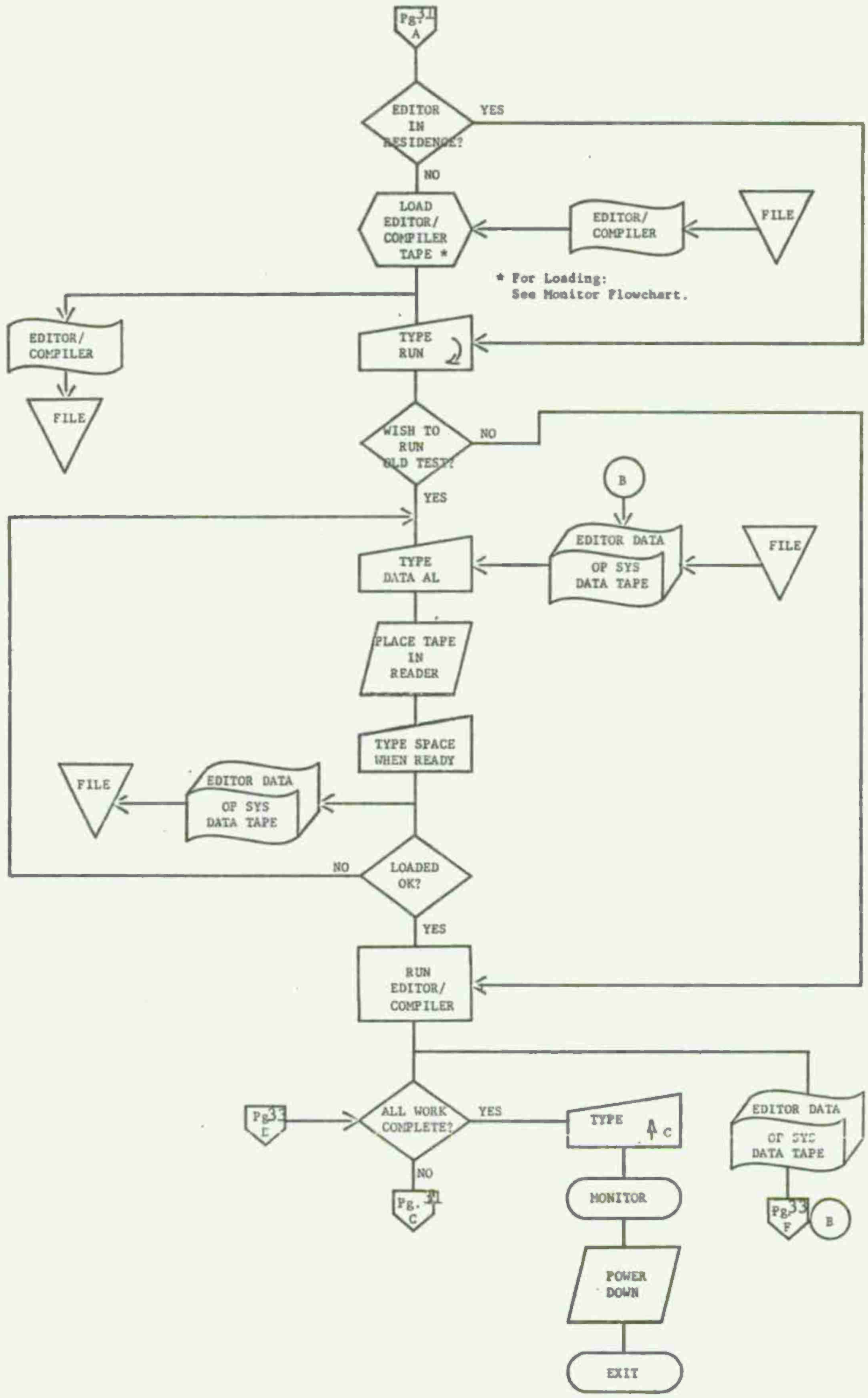
	DECISION The decision function is used to document points in the system where a branch to alternate paths is possible based upon variable conditions.		INPUT/OUTPUT Any type of medium or data.
	PREDEFINED PROCESS A group of operations not detailed in the particular set of flowcharts.		PERFORATED TAPE Paper or plastic, chad or chadless.
	TERMINAL The beginning, end, or a point of interruption in a system.		DOCUMENT Paper documents and reports of all varieties.
	SAME PAGE CONNECTOR An entry from, or an exit to, another part of the system flowchart on the same page.		OFFLINE STORAGE Offline storage of either paper, cards, magnetic or perforated tape.
	OFFPAGE CONNECTOR A connector used instead of the connector symbol to designate entry to or exit from a page.		ONLINE KEYBOARD Information supplied to or by a computer utilizing an online device.
	FLOW DIRECTION The direction of processing or data flow.		CLERICAL OPERATION A manual offline operation not requiring mechanical aid.
	ANNOTATION The addition of descriptive comments or explanatory notes as clarification.		KEYING OPERATION An operation utilizing a key-driven device.
	PROCESSING A major processing function.		AUXILIARY OPERATION A machine operation supplementing the main processing function.

In each of these blocks, further information is usually given to aid the explanation of the block. Flowcharts are normally read from left to right, and down. If the flow is from right to left or up, arrows are used to indicate the change. Two blocks are used as connectors; they are:  and . The  indicates a same page connector. This symbol contains a letter and connects a block with the same connector and letter. The  is an off page connector. It usually contains the page number where the corresponding connector is located. Under the page number is a letter (s) to match with the corresponding connector. The corresponding connector contains the page number which referenced this connector.

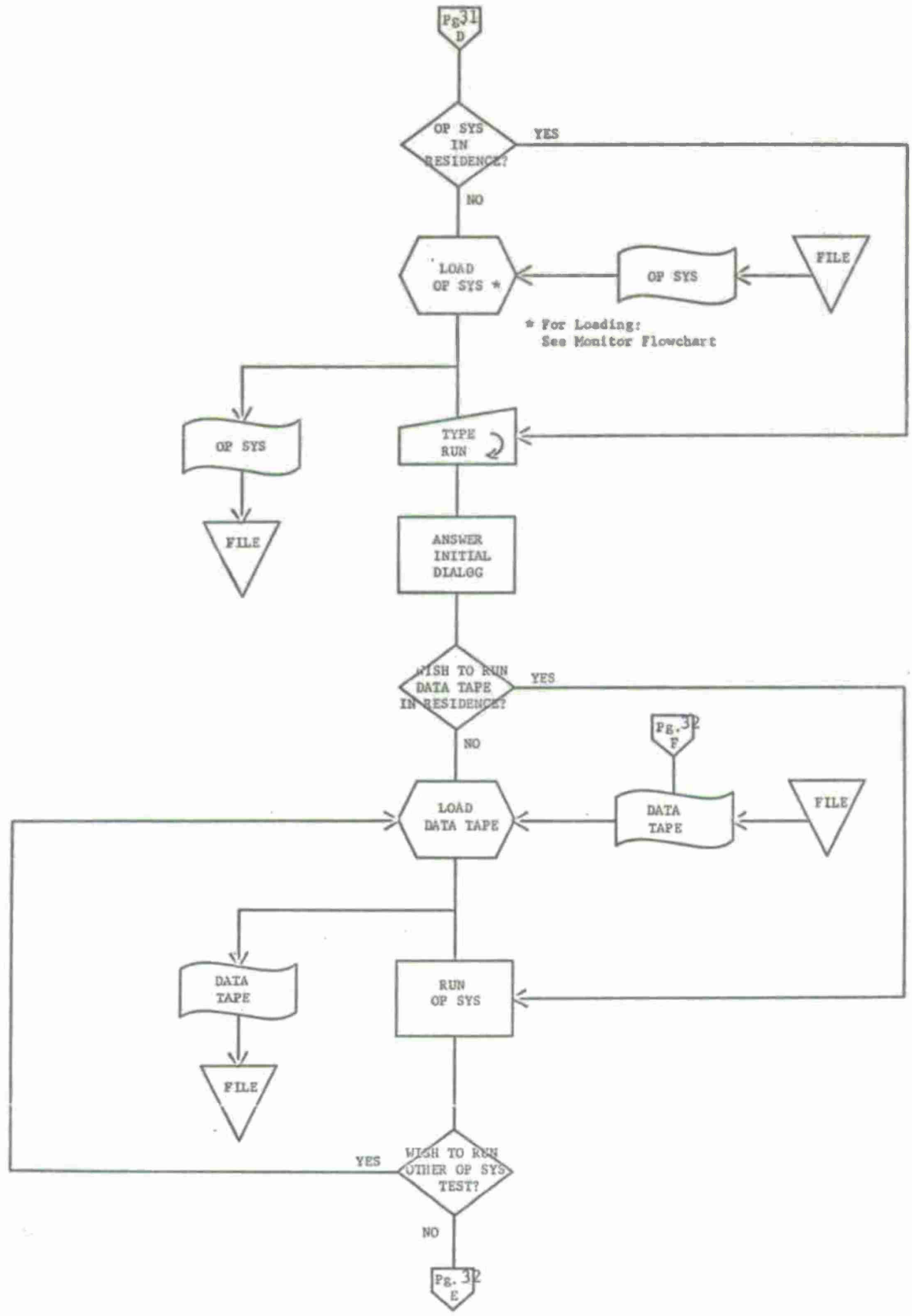
SYSTEM FLOWCHARTS



SYSTEM STARTUP

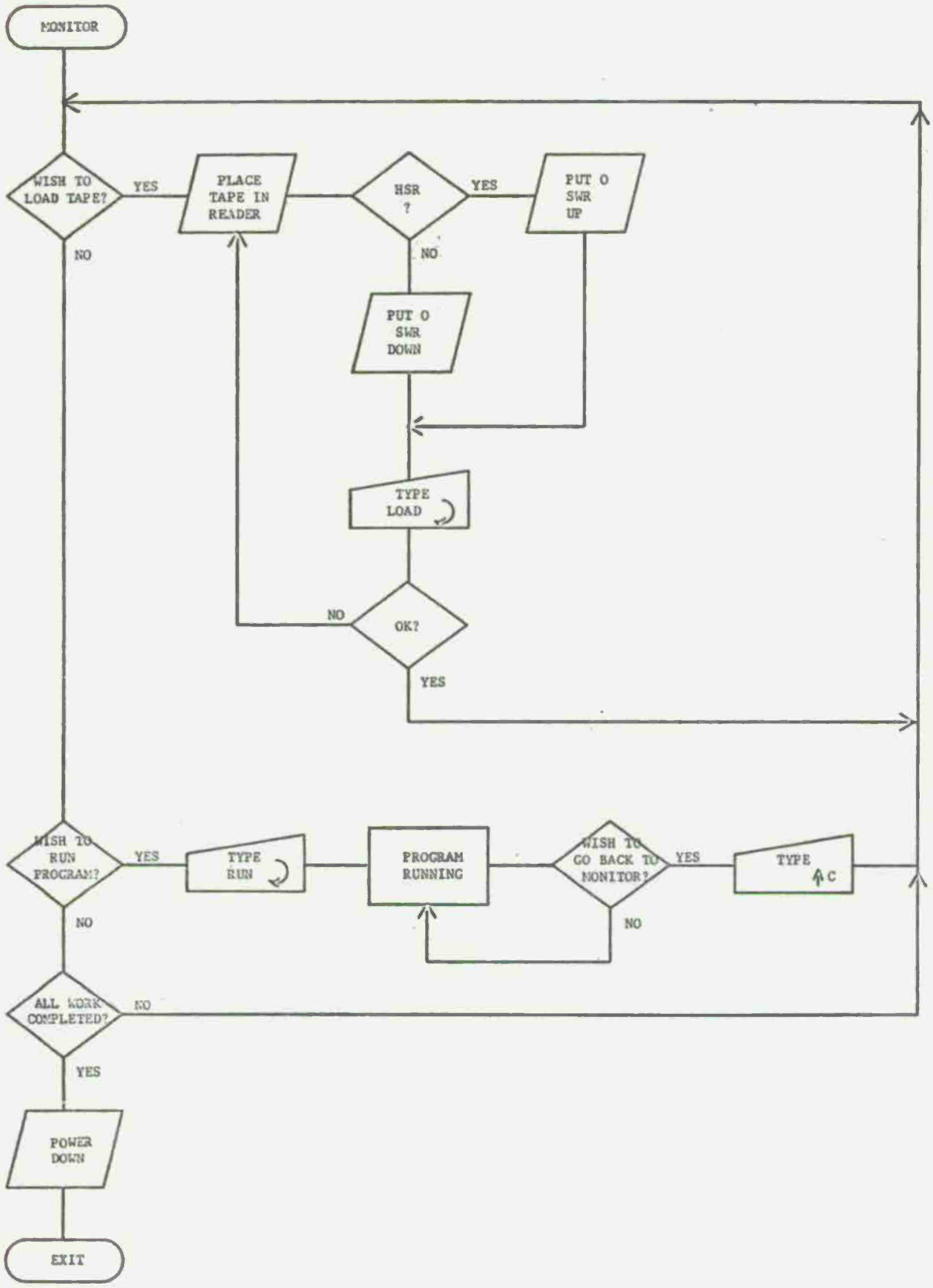


EDITOR/COMPILER



OPERATING SYSTEM

MONITOR FLOWCHART



5. MINIMUM SYSTEM HARDWARE

This section summarizes the minimum electronic hardware required to perform an automatic sine-sweep test. The equipment is described according to its funtional role in the control loop—such roles as feedback signal conditioning and multiplexer A/D converter. The equipment configuration delineated herein consists of the T5001 system, as this setup was used in the evaluation effort. However, the control concept behind this setup applies to any digital control design of dynamic testing.

Also presented for general information are the typical performance characteristics of the individual elements of the T5001 system.

5.1 Feedback Signal Conditioning

(1) The system includes a fully compatible digitally controlled signal conditioning system for piezoelectric tranducer.

(2) The analog conditioning uses a regulated voltage low-impedance system, usable with any two-wire signal cable.

(3) The system includes an impedance converter (line driver) system, a digitally controlled scaling amplifier, a digitally controlled normalizing amplifier, and a digitally controlled true rms (square law) signal processor system (D701, D710, D726 modules).

(4) The line-driver unit is available with either *charge* sensitive or *voltage* sensitive inputs, and has a micro-dot input connector and a BNC output connector. The line-driver-output impedance is less than 1 Ω.

(5) The scaling amplifier (D701) has the following performance specifications:

   (a) Gain is controlled and read by a binary exponent, so that 2^2N is the amplifier gain and N is the binary number used to control and read the gain.

   (b) The amplifier has six gains, 1, 4, 16, 64, 256, 1024 that are controlled by the exponent N = 0, 1, 2, 3, 4, 5.

   (c) The amplifier has a dynamic range of at least 60 dB, except as limited by system noise, on all gain ranges.

   (d) The amplifier has a broad-band noise level of less than 6 μV referred to input.

   (e) The amplifier has a broad-band frequency response (3-dB points) of 0.2 to 20 kHz.

(f) The amplifier has a linearity of at least ±1 percent and a gain accuracy of 1 percent of full-scale output.

(g) The amplifier input uses constant voltage low-impedance zero-drive conditioning techniques, and permits the use of both voltage and charge-sensitive transducers.

(6) The normalizing amplifier (D710) is a high-input impedance amplifier compatible with the scaling amplifier. The normalizing amplifier is capable of normalizing transducers, having sensitivities in the range of 1 to 1000 μV or pico-coulombs per unit, to 1 percent of point accuracy. The normalizing amplifier gain is under control of a binary word using a floating point format of the form $Y = X2^N$, where $0.5 \le x \le 1$ and $0.0 \le N \le 7$. The fraction x is expressed with 7-bit accuracy and the exponent N is expressed with three bits.

(7) The signal processor module (D726) is compatible with the performance of the signal scaling and signal normalizing amplifiers. The signal processor provides true rms detection of the feedback control signal using square-law detection techniques.

(8) The signal conditioning system includes a universal module rack wired to control up to eight modules via binary-control signals, and provides input and output connections for up to eight analog signals via BNC connectors. This enables the computer to supervise up to eight separate accelerometers.

5.2 Multiplexer and A/D Converter

The output of the signal-processor module (D726) is input to a multiplexer and A/D converter system. The multiplexer has sufficient inputs to permit seven additional signal conditioning channels to be added for signal selection and averaging control.

The AD converter meets the following performance:

(a) Word length: 12 bits

(b) Sample rate: computer controlled to 40 kHz

(c) Sample and hold aperture: less than 50 nsec.

For a detailed description of how an A/D converter reads data, refer to section 6. For acceptable sine-sweep test data rate, refer to section 7.11.

5.3 Digital Processor (PDP-11)

The digital processor contains a minimum of 8092 words of 16-bit read/write memory with a cycle time of 1.2 μsec.

(1) The memory is expandable in 4096-word blocks to 32,768 words total.

(2) The processor is capable of directly addressing up to 32,768 words.

(3) All processor functions (arithmetic unit, memory, input/output) and all external devices are on a common parallel data bus.

(4) The processor has a four-level priority interrupt structure. The interrupt structure has a nominal response time of 7.2 μsec.

(5) The processor has instruction for manipulating both 8-bit and 16-bit words.

(6) The processor has an ASR-33 teleprinter and interface. The teleprinter includes a 10-Hz paper tape reader and punch. The real-time printout rate of this teleprinter is limited to approximately 3 octaves/min.

5.4 Signal Synthesizer (D800)

The sine-wave signal synthesizer uses digital techniques to synthesize a sine wave and is under direct processor control.

(1) The sine-wave synthesizer uses a floating point binary number that is directly equal to the analog frequency. The floating point number is of the form $Y = .X2$ where $0.5 < x < 1$ and is expressed in 10 + 1 bits. The exponent N is expressed in 4 bits.

(2) The synthesizer is programmable over a frequency range of 0.5 Hz to 16 kHz. The frequency programming and control has an accuracy of 0.1 percent of point.

(3) The analog sine-wave distortion components are less than 0.5 percent.

(4) The synthesizer has a cosine wave output which lags the sine wave by 90 ±1 deg.

(5) The sine-wave synthesizer has an optional dc voltage output which is proportional to frequency.

5.5 Amplitude Control Precision Amplifier (D711)

The system amplitude control is accomplished by this digitally controlled analog amplifier.

(1) The amplifier is programmable using a floating point command proportional to the gain.

(2) The command word is of the form $Y = .X2^N$ where $0.5 < x < 1$ is expressed in 7 bits and N is expressed in 4 bits.

(3) The amplifier has a programmable range of 96 dB and a minimum analog dynamic range of 60 dB.

5.6 Paper-Tape Reader/Teleprinter

The system includes a paper-tape reader and interface capable of reading punched tapes at speeds up to 300 Hz. The reader is capable of reading both eight-level ASCII and full binary data.

The teleprinter is used for all communications between the operator and the computer. The ASR-33 teletype provides a field of 72 characters.

5.7 Physical Environmental Requirements

(1) The test system is contained in one standard 19-in. cabinet. The cabinet occupies no more than 9 sq ft of floor space and is less than 80 in. high.

(2) Utilities

The control system operates on 115 V ±10 percent, 60-Hz single phase power.*

(3) Temperature

The system operates in a temperature environment of 0° to 35°C.

(4) Humidity

The system operates in from 0 to 95 percent relative humidity.

6. ANALOG-TO-DIGITAL AND DIGITAL-TO-ANALOG CONVERTER

6.1 Technical Operations

The A/D converter is a device intended to map a continuous (analog) voltage signal into the corresponding discrete integer numbers. The most commonly used number representation consists of binary steps of 2^n, where n is an integer. The conversion is intended to provide a method for reliably and accurately storing, transmitting, or operating upon such analog voltage signals. In data processing as well as in communications.

**Shaker/power amplifier utilities not included.*

digital data are usually expressed in binary form; hence, the most common but by no means the only representation of a digitized voltage signal is the binary representation.

Figure 2 diagrams the typical operation of the A/D and D/A converter. The input data are sampled at equal time intervals (t=nT), and is automatically being converted into a sequence of numbers that can be recognized by the digital processor. The reverse procedure must take place for the processor to communicate back with the data source. Here

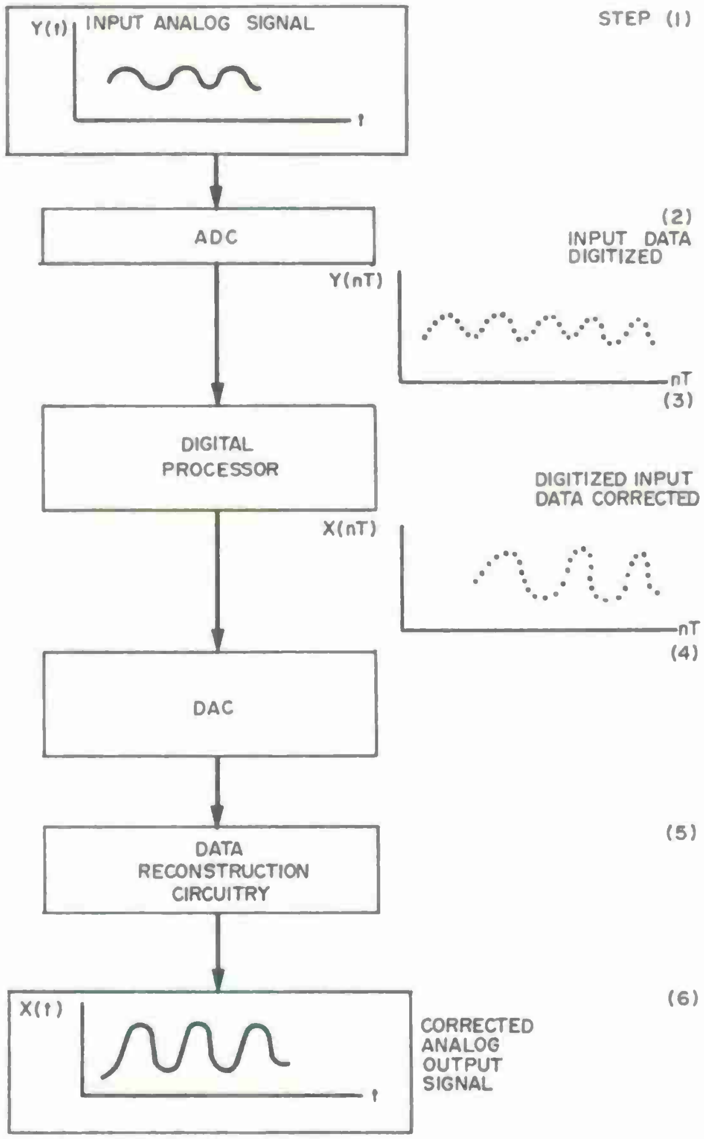


Figure 2. Typical analog-to-digital and digital-to-analog conversion process.

a sequency of binary numbers is converted into an analog signal of the form X(t) by the D/A converter and appropriate reconstruction circuitry. Provisions could be made to optimize the data sample rate for a variable source frequency.

6.2 Binary Number Representation and Quantization Error

Whenever an analog signal is converted into a digital form, a quantization error(s) will result from the use of a finite number of integer digits. The number of digits to be used depends on the maximum acceptable quantization error. The A/D and D/A converters of this DDC test system use 10 bits A/D and D/A conversion techniques. Using such techniques, the data field is divided into $1023(=2^{10}-1)$ points. This would yield a resolution of ±1/2 of the least significant bit anywhere in the field or a maximum error of about 0.5/1023, which is less than 0.05 percent.

The binary representation of a number is achieved by dividing the data field into counts made up of powers of 2. In binary notations using a 10-bit word format, the count 0 and 1023 can be represented as:

$$(0\ 0\ 0\ 0\ 0\ 0\ 0\ 0\ 0\ 0)_2 = 0$$

$$(1\ 1\ 1\ 1\ 1\ 1\ 1\ 1\ 1\ 1)_2 = 1023$$

Any count between 0 and 1023 can therefore be expressed as a serial combination of binary 0 or 1 as described below:

BIT NO. (N)	10	9	8	7	6	5	4	3	2	1
VALUE IN POSITION	$(X)2^9$	$(X)2^8$	$(X)2^7$	$(X)2^6$	$(X)2^5$	$(X)2^4$	$(X)2^3$	$(X)2^2$	$(X)2^1$	$(X)2^0$

where for

X = 1   Value of 2^N counted

and

X = 0   Value of $2^N = 0$

N = 0, 1, 2, 3, 4, 5, 6, 7, 8, 9.

The numerical count (actual value of the number is obtained by summing the nonzero powers of 2.

$$\text{Numerical Count} = \sum[(X)\cdot 2^0 + (X)\cdot 2^1 + (X)\cdot 2^2 + \cdots (X)\cdot 2^9]$$

The binary number $(1\ 0\ 1\ 0\ 0\ 0\ 0\ 1\ 1\ 1)_2$ is read as follows:

BIT NO. :	10	9	8	7	6	5	4	3	2	1
	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓
VALUE IN POSITION:	1	0	1	0	0	0	0	1	1	1
	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓
NUMERICAL VALUE:	$(1)2^9$	$(0)2^8$	$(1)2^7$	$(0)2^6$	$(0)2^5$	$(0)2^4$	$(0)2^3$	$(1)2^2$	$(1)2^1$	$(1)2^0$
	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓

$$\text{NUMERICAL COUNT} = \sum[512 + 0 + 128 + 0 + 0 + 0 + 0 + 4 + 2 + 1] = 647$$

Based on a total voltage range of say 1.000 V, count zero represents 0.000 V and count 1023 = 1.000 V. Numerical count 647 is therefore equivalent to 647/1023 = 0.623 V. (For a voltage range of 1.023 V, this quantity would be equivalent to 647 × 1.023/1023, or 0.647 V.)

Table II presents a summary of the standard 10 bits binary-to-decimal conversion code.

TABLE II. STANDARD 10 BITS CONVERSION CODE FOR BINARY NUMBERS

Bit No.	Bit value	Ratio	Numerical value for total range of 1.023 V
10	512	$\frac{\text{Decimal Range}}{1023}$	.512
9	256	"	.256
8	128	"	.128
7	64	"	.064
6	32	"	.032
5	16	"	.016
4	8	"	.008
3	4	"	.004
2	2	"	.002
1	1	"	.001
	$\sum = 1023$		$\sum = 1023$ V

7. DIGITALLY CONTROLLED ELECTRODYNAMIC VIBRATION SYSTEM FOR SINE TESTING—TECHNICAL CONSIDERATIONS*

7.1 Digital-Control Concept

A new vibration test method is currently being implemented for sine testing. The conventional analog equipment used in sine-sweep testing is replaced by a small digital computer and associated peripheral hardware and software. The purpose of the digital system is to obtain a complete automatic control of the sine sweep or dwell test from power up, through testing, to shutdown. No human intervention is required during the test, and only minimal programming is required to prepare the test, a concept that optimizes reliability and safety. The new digital-control system is designed to carry out the control task of the conventional analog equipment but with increased reliability, accuracy, speed, and safety. Other major benefits that can be derived from a digital control system are the substantial cost savings resulting from reduced setup time for production tests, as well as the utilization of the mini-computer as a real-time test data analyzer/documenter. With added peripherals, the typical control system is capable of analyzing data from a total of eight channels (test points).

The specific sine test is programmed before actual testing through a conversational routine. This program language is simple, does not require extensive knowledge of computer programming, and is designed specifically for vibration testing. It is organized around a logical sequence of questions in the English language. The operator answers these questions by typing on a keyboard. With this method, the classical "forgotten switch" problem no longer exists.

After all test parameters (such as amplitudes, frequencies, sweep rate, and control limits) are entered, a hard copy in the form of a paper-data tape (or other forms of hard copy) is generated to run the particular sine test. The same data tape(s) could be used over and over to repeat the same test(s), thereby virtually eliminating test setup time. In addition, an on-line test modification technique can be used to create new test mode(s) on real-time basis.

The final configuration of the digitally controlled vibration system consists of the computer and its peripherals. No front panel controls are used. All test parameters are fed in via paper tape, and the computer carries out the complete test mode without human intervention. Control limits are imposed on any of the specified test levels, and the computer will automatically terminate the test if these levels are exceeded to insure adequate protection of the test specimen. The control (reference) accelerometer can be placed at the input or any relative test point on the specimen. During debugging operations, the exciter system is uncoupled from the control loop.

**Selected paragraphs from ref. 1 were included in this section for the convenience of the reader.*

7.2 Dynamic Range Considerations

One of the most important parameters to be considered in the design of a digital control system is the range of values required to perform a general sine test. This parameter can be determined by investigating the limits of a typical sine test. The frequencies encountered range from 5 to 3000 Hz for general work. (The frequency extremes can be less than 1 Hz for electrohydraulic vibrators to greater than 15,000 Hz for acoustic exciters.) The vibration amplitudes are also subject to wide variations. The required vibration on the exciter may typically range anywhere from 0.1 to 300 g. The required drive to the exciter may range even further due to resonances in the exciter response. In general, a high degree of accuracy is needed in holding the required vibration level and an even higher accuracy is required for frequency resolution. An analysis comparing three of the most used methods of representing a number (i.e., fixed point, floating point, and logarithmic) shows that the best number system for sine-test requirements is the floating point (scientific) notation. This is the number system selected for the digital sine-control concept in both the computer and the peripheral equipment (see analysis in sect 7.9).

The use of floating point arithmetic in a computer can seriously slow down its reaction time. Two things are required to avoid excessive speed reduction. The first is the selection of a fast computer with a well organized instruction set. The second parameter is the development of high-speed floating point algorithms. These algorithms are required in the high-data rate portions of the sine-control system.

The first requirement can be satisfied by the selection of the PDP/11 computer or an equivalent type. The second requirement can be met by performing a careful analysis of the speed requirements of sine control work and then generating control algorithms and hardware to exactly match these requirements.

7.3 Control Computer

The central control computer forming the heart of the sine-control system is the new (4th generation) 16-bit PDP/11-20 manufactured by Digital Equipment Corporation. Its unibus architecture makes it the ideal computer for the required application. Its speed and flexibility give it the ability to meet the exacting requirements of vibration testing. The data frequencies involved in sine testing dictate the need for speed. The very wide dynamic range inherent in the application, forcing as it does the use of floating-point arithmetic, dictates the need for computer flexibility as well as speed.

Another important consideration in the selection of the PDP/11 is the ease with which it fits in with the building-block approach described in succeeding sections. For example, one can start off with a simple

sine-control system, and increase its capability at any later date to include random or analysis capabilities simply by plugging in the new peripherals.

7.4 State-of-the-Art Analog Test Equipment

To fully comprehend what must be implemented to achieve direct digital control of dynamic testing, the conventional analog test control technique and associated design problems are reviewed.

The heart of an environmental test laboratory supporting electromechanical design, development, and production/qualification testing, is the electrodynamic vibration exciter. Force, displacement, and electrical power are the most important design parameters for such exciters. These parameters result in a far from flat transfer function characteristics for the exciter. A typical acceleration characteristic is illustrated in figure 3, where the ratio of bare table acceleration ($\ddot{X}$) to driving voltage (Vd) is plotted versus frequency. However, interactions between load and exciter (i.e., such as fixture resonance) can effect this characteristic considerably (see dashed line). The principal requirement of any control system, be it digital or analog, is to automatically compensate for the transfer function of the load and exciter. A block diagram of present day analog control system is presented in figure 4. To simplify the discussion, only the one channel AVD (acceleration, velocity, displacement) version is shown. There are two areas in this block diagram of special interest as far as a digital control is concerned. One area is associated with the feedback detector used to obtain the amplitude information. The other area is in the region where the typical acceleration signal is passed through integrators to get AVD control.

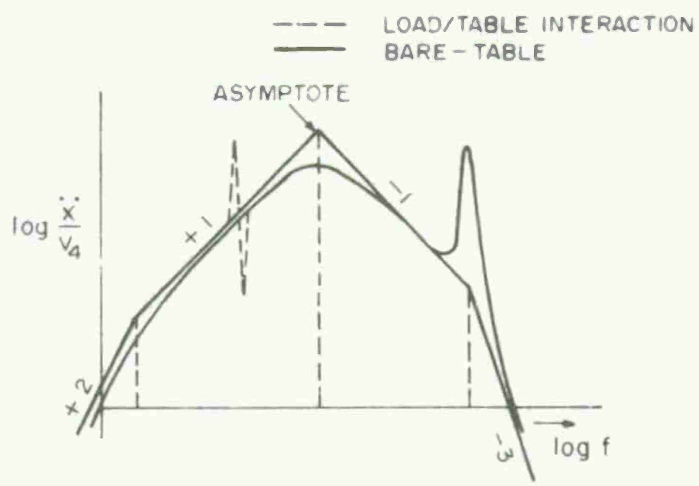


Figure 3. Acceleration to driving voltage ratio versus frequency.

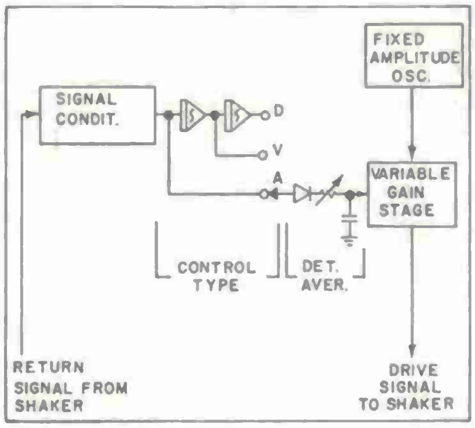


Figure 4. Block diagram for single-channel analog control test equipment.

In general, detectors in use today are of the average type. The rectified signal from the detector is passed through a low-pass filter to obtain the optimum control-loop slewing speed with the minimum amount of distortion due to rectification effects. The user wants to control his acceleration using one of two parameters: (1) peak acceleration (g) or (2) rms acceleration (g). However, usually both peak g and g rms are based on the definition of the average detected value of a sine wave at the shaker frequency. The output of the detector is the average of the input signal; this means that not only is the fundamental detected but any noise or harmonic distortion on the input is also sensed. The action of the detector can then be briefly described as follows: The detector senses the average of the magnitude of the wide-band input (return) signal, with the averaging time adjustable over a wide range.

The signal conversion circuits (converting from acceleration to velocity or to displacement) serve two purposes. The first purpose is to yield for an acceleration input signal, a real-time output signal of the velocity or of the displacement. In the process of generating a velocity or a displacement from acceleration, any high-frequency noise present on the acceleration signal is reduced. The circuits used to generate the velocity and displacement signal are generally not pure integrators but act as low-pass filters with their break frequencies below the exciter operating frequency. One of the general problems inherent in the use of integrators is that they tend to magnify low-frequency noise. In high-quality sine-control packages, this low-frequency noise problem is reduced by placing a high-pass filter in the signal path before the integrators, with its corner frequency tracking the audio frequency. The essential ingredients of the AVD signal conditioner can now be described. The AVD signal conditioner is composed of one or two low-pass filters with cutoff frequencies somewhat below the exciter operating frequency; and in high-quality situations, tracking high-pass filters are crudely slaved to the operating frequency to reduce low-frequency noise. Also, the low-pass filters tend to reduce

high-frequency effects that could be present on the acceleration signal. Since the overall effect of a combination high-pass and low-pass filter is a bandpass filter, the signal converter circuit appears to be a special case of a tracking filter.

The next problem of complexity in designing an analog sine-control system is consideration of the requirement for controlling the level of only the fundamental on the shaker table. Usually, a tracking filter is added to the system block diagrammed in figure 4. The tracking filter is placed in the signal path before the signal-conversion circuits. Essentially, the tracking filter eliminates the harmonic distortion and noise present on the raw acceleration signal. In this type of application, even though the detector is wide band, it has only the fundamental component presented to it. Therefore, the feedback system controls to the level of the fundamental only. Any noise or harmonic distortion has no effect on the control. One point of importance that must be considered with the addition of the tracking filter is that the filter tends to reduce the stability of the control system—the allowable compressor speed has to be much slower than is permitted for the wide-band system.

7.5 Amplitude Control

It is essential in planning a direct-digital sine-control system to arrange for the computer itself to perform every function possible, limited only by the maximum input-data rate that the computer can handle.

If the system is planned correctly, the computer plus a few basic peripherals can be programmed to cover all sine-control situations. These situations include such parameters as those involving phase control, tracking, averaging, signal selection, resonant search and dwell and narrow-band random. All that is needed is the appropriate software. A new situation can be set up in a matter of minutes.

The digital-control system achieves maximum flexibility by digitally processing all analog feedback and forward signals which were described in section 7.4. Complete amplitude control of the analog signal is thus achieved digitally. Refer to section 7.7 for detailed discussion of digital control of test amplitude using a wide-band and tracking filter techniques.

7.6 Frequency Control

In the analog system, the frequency is generally swept through time from one of the frequency extremes to the other extreme in a logarithmic manner. This sweep type is used to achieve a constant-Q sweep. Here the percentage change in frequency with time is constant. With a constant-Q sweep, resonances in the exciter/load combination are vibrated equally for a sharpness of resonance below a certain critical number dependent on the actual sweep speed. Section 8 discusses in detail the digital-control technique meeting the requirements for frequency control.

The typical range of sweep speeds is from 2.0 to 0.01 decades/min (approx 6.7 to 0.035 octaves/min). The DDC system in operation at HDL is programmed for a range of 7.0 to 0.1 octaves/min, as most applications fall well within this range. However, higher sweep speeds, in excess of 10.0 octaves/min, are currently under development.

7.7 Sweep-Sine Digital Control System Configuration—Tracked/Untracked Modes

7.7.1 Overall Operations and Description

With the results of the analog analysis in mind, the final swept sine configuration can be described. Figure 5 block diagrams the basic system hardware. All (peripheral) devices are controlled by the computer; also, they can communicate with it when commanded.

This signal conditioner accepts the acceleration return signal from the shaker. Through computer control, the signal is conditioned to present the proper voltage to the A/D converter. The digital output of the A/D converter is then brought into the computer where a measure of the correctness of the shaker vibration level is made. The computer then makes an amplitude correction decision. It then performs a digital-filtering operation on the error correction. The gain of the variable gain stage is then adjusted to retire the amplitude error, thereby closing the feedback loop.

The frequency is swept by sequentially incrementing (in a logarithmic manner) the digital-frequency-command number. This is done in very small increments. This number is then transmitted to the digital oscillator.

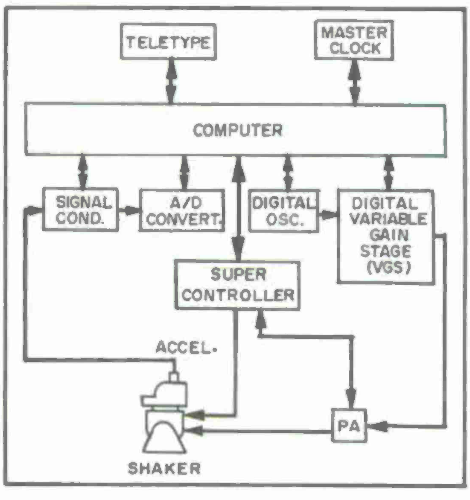


Figure 5. Block diagram of direct-digital control system hardware.

With this basic system, a multiple level program is easily handled. In the nonoperating data acquisition phase of the program, any arbitrary group of acceleration, velocity, or displacement sections (as a function of frequency) can be programmed. This feature allows the operator to specify an amplitude versus frequency versus time curve to properly fit almost any sine-test requirement.

There are several more complicated sine-system requirements of common usage. One of these requirements is to accept multiple return signals from the exciter and load. The total vibration level is then controlled according to one of a number of defined rules regarding the formation of a composite signal to be used for control. One rule requires us to control to the average of the sum of the return signals. The other rule sets control of the vibration level to the highest of the return signals. In the digital sine control system, this is achieved by providing—in hardware—one signal conditioner for each return signal. A multiplexer then sequentially samples each signal through the A/D converter. The computer software package is then extended to account for the additional return signals.

The master clock acts as the computer time base, thereby allowing accurate control of the rate of frequency sweep, effective amplitude correction rate, and total testing time.

The teletype acts as the primary communication link between the operator and the system. The use of a teletype as an integral part of the system has several advantages. This use centralizes all the control functions into one device. With the language, the printer displays appropriate questions in an easy-to-read format. It then displays the answers as typed on the keyboard. During the test run, the status of the system and the validity of the test is printed out; and with this printing feature, a permanent record of the test is obtained for each run. This hard copy can be used as documentation of the test for future reference.

The supervisory controller acts as the hardware system controller and as the system safety monitor. Upon computer command, the controller produces the proper analog signals required to cycle amplifier system to ready condition. The controller also converts amplifier/shaker status information in such forms as pressures, temperatures, interlocks, into a digital format suitable for the computer. The computer continuously checks these status signals and takes appropriate action if required.

The total system control is then set up as before, through the special conversational language.

7.7.2 Untracked Mode

In the untracked operating mode, the sinusoidal excitation of the shaker is controlled to the overall rms level of the return signal, which consists of the fundamental content of the signal, harmonics of the fundamental, as well as extraneous noise. Therefore, although the test

amplitude can be satisfied, it is necessarily satisfied at a single frequency. Control to a precise frequency can be assured only when contributions from all harmonics and noise sources have been filtered out. This technique is described in section 7.7.3 below.

Figure 6 shows schematically (switch position 1) how tracked and untracked control are executed. In the untracked mode, the feedback signal (V_{in}) is fed into the processor/multiplier (D726 unit) for square-law detection. The input is then multiplied by itself to yield a $\sin^2(x)$ type signal (at twice the incoming frequency), with positive ordinates only. Let the return signal be characterized by V_{in} as expressed below in equation (1).

$$V_{in} = C \sin(wt + \alpha) + \sum_{n=2}^{m} Cn \, Sin\,(n\,wt + \alpha n) + er \qquad (1)$$

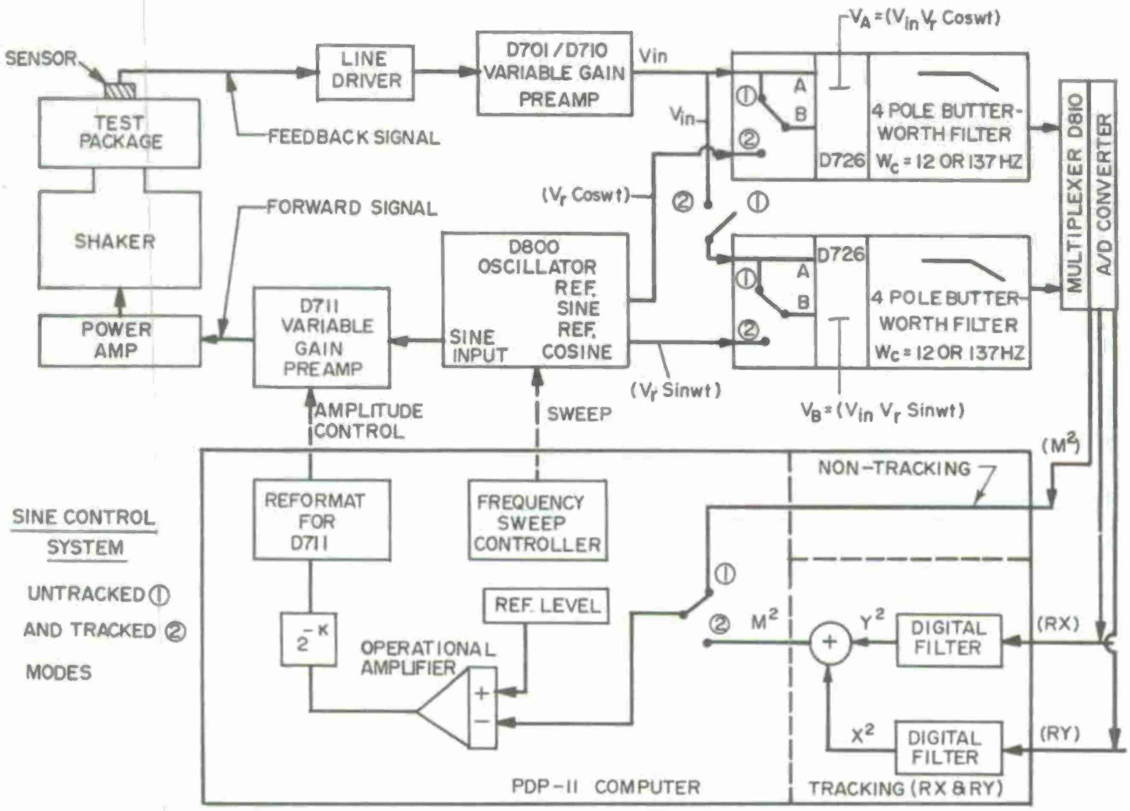


Figure 6. Block diagram for tracked and untracked digital control.

where:

V_{in} = Transducer output (~V)

$C \div Cn$ = Fundamental and harmonics components of shaker amplitudes (~V)

W = Driving frequency (~Hz)

α = Phase angle (~rad)

n_1m = Index

er = Random noise (~V)

Let V_{in} = M

$$M^2 = C^2 \sin^2(wt + \alpha) + \sum_{n=2}^{m} Cn^2 \sin^2 (nwt + \alpha n) + e_r^2$$

$$2C \sin (wt + \alpha) + Zer \sum_{n=2}^{m} Cn \sin(nwt + \alpha n)$$

Noting that for nw $\geq$ 12.4 (i.e., w $\geq$ 6.2 Hz), the signal will be attenuated by a 4-pole Butterworth (low pass) filter at a rate of approximately 24 dB/oct.; and that when w $\geq$ 12.4 Hz all oscillatory content is filtered out, this above expression can be reduced to:

$$M^2 = C^2 \sin (wt + \alpha) + \sum_{n=2}^{m} Cn^2 \sin (nwt + \alpha n) + e_r^2 \cdot$$

The trigonometric identity $\sin^2 X = \frac{1 - \cos 2x}{2}$ can be used to further simplify the expression for M.

$$M^2 = \frac{C^2}{2} [1 - \cos 2(wt + \alpha) + 1/2 \sum_{n=2}^{m} Cn^2 [1 - \cos 2(nwt + \alpha)] + e_r^2$$

$$= \frac{C^2}{2} + 1/2 \sum_{n=2}^{m} Cn^2 + e_r^2 \; \frac{C^2}{2} [\cos 2(wt + \alpha)] + \sum_{n=2}^{m} \frac{Cn}{2} [\cos(nwt + \alpha n)]$$

As all oscillatory content is being filtered out,

$$M^2 = \frac{C^2}{2} + 1/2 \sum_{n=2}^{m} Cn^2 + e_r^2 \tag{2}$$

Thus, the return signal consists of contributions from the fundamental amplitude (C), harmonics of the fundamental amplitude (Cn), and random noise (e_r).

As the test frequency increases, faster response (or lower time constant filter) is required to maintain real-time control. At 68.5 Hz, for which the harmonic component is equal to 137 Hz, another 4-pole Butterworth bandpass filter is introduced, with at least 50-dB attentuation at this frequency. The amplitude filtering process is therefore maintained void of any oscillatory content, although the amplitude square quantity (M^2) is the net resultant of *all* existing frequency components. For test frequencies between 5 and 6.4 Hz, a software filter is employed as the process is relatively slow. Consequently, the net effect here is to produce a true rms amplitude quantity (M^2) before the square root is extracted, an output that has an equivalent dc representation. The output of the D726 unit is then periodically sampled by the A/D converter at the constant sampling rate of 512 samples/sec. Each sampled value, defined as (M^2), is initiated by a clock-generated interrupt.

The output of the A/D converter (M^2) is fed into the computer where the measure of the correctness of the signal is ascertained. The computer has already been programmed for the desired test level (REF), and the quantity ($REF-M^2$) is generated for each sample, continuously integrated over time (INT) and stored. The integration is performed K times, yielding ($INT/2^k$); this quantity is reformatted to increase or decrease the gain of the forward gain amplifier (D711 unit), depending if the quantity ($INT/2^k$) is negative or positive. For example, if ($REF-M^2$) is positive, $REF > M^2$ and ($INT/2^k$) is increased. Since the forward gain amplifier is directly proportional to INT, the signal to the exciter will be increased to retire the error so that ($REF-M^2$)$\rightarrow 0$. This will result in increased excitation of the test package. The opposite process will take place if the return signal proves higher than was requested.

The quantity K is the compression factor that controls the dynamics of the control loop. It must be carefully selected on the basis of test frequency, sample rate, and interaction due to resonance. Too small a K could ultimately result in overcontrol, whereas too large a K could lead to loss of control. The selection of K, however, is accomplished automatically by the system.

7.7.3 Tracked Mode

The primary reason for using a tracking filter is to supply the digital control system with information contained with the fundamental frequency of the input signal only. This insures that the desired test level, at a specific frequency, will be satisfied regardless of existing harmonics or noise. However, since the contribution from these harmonics are muted out in this process, the actual test level may be significantly higher than intended.

The filtering process adapted here is essentially a mathematical operation that extracts the fundamental component only. This permits the computer to control the test amplitude to the precisely desired frequency; no side-band contributions characteristic of the analog filter exist.

Referring to switch position No. 2 in figure 6, the tracked mode is implemented by feeding the return signal into two separate signal processors/multiplier units (D726). In one such unit (A), the feedback signal is multiplied by a reference sine wave from the digital oscillator (D800 unit), and in the second D726 (B) by a reference cosine wave 90 deg out of phase. The output voltage from each processor/multiplier unit is given as:

$$V_A = V_{in} \, Vr \cos wt \tag{3}$$

$$V_B = V_{in} \, Vr \sin wt \tag{4}$$

The feedback signal from the control accelerometer can be expressed as:

$$V_{in} = \underbrace{C \sin (wt + \alpha)}_{\text{fundamental content}} + \sum_{n=2}^{n=m} \underbrace{Cn \sin (nwt + \alpha n)}_{\text{harmonic content}} + \underbrace{Er}_{\text{noise}} \tag{5}$$

where

- w ~ driving frequency
- Vr ~ reference voltage
- V_{in} ~ total feedback signal voltage
- t ~ time
- α ~ phase angle $\quad (0 \leq \alpha \leq 180°$
- C ~ amplitude of fundamental signal
- n ~ index

Note that the feedback signal consists of a fundamental component at a total frequency of $(wt + \alpha)$ to account for possible phase shifts at the shaker, as well as components due to harmonics and extraneous noise.

When V_{in} from equation (5) is substituted into equations (3) and (4), the value of the output voltage becomes

$$V_A = (VrC) \cos wt \sin(wt + \alpha) + Vr \cos wt \left[\sum_{n=2}^{n=m} Cn \sin(nwt + \alpha n) + Er \right] \quad (6)$$

$$V_B = (VrC) \sin wt \sin(wt + \alpha) + Vr \sin wt \left[\sum_{n=2}^{n=m} Cn \sin(nwt + \alpha n) + Er \right] \quad (7)$$

given the trigonometric identities

$$\sin x \cos y = 1/2 \sin(X + Y) + 1/2 \sin(X - Y) \qquad x = wt + \alpha$$

$$\sin x \sin y = 1/2 \cos(X - Y) - 1/2 \cos(X + Y) \qquad y = wt\ .$$

Equations (6) and (7) can be rewritten as

$$V_A = \frac{VrC}{2} [\sin \alpha + \sin(2wt + \alpha)] + (\text{remaining terms}) \quad (8)$$

$$V_B = \frac{VrC}{2} [\cos \alpha - \cos(2wt + \alpha)] + (\text{remaining terms}) \quad (9)$$

where remaining terms consist of the reference sine or cosine wave multiplied by the contributions from frequencies, harmonics, or extraneous noise. Thus, the periodic value of all remaining terms averages to zero. Using a low-pass filter (analog 4-pole Butterworth and digital filter), the extracted components are expressed by equations (10) and (11) as follows:

$$\left| V_A = \frac{VrC}{2} \sin \alpha \right| \quad (10)$$

$$\left| V_B = \frac{VrC}{2} \cos \alpha \right| \quad (11)$$

Equations (10) and (11), designated as RY and RX in figure 6, represent the Y and X components of a vector whose magnitude is proportional to the test amplitude. The RY and RX components are fed from the A/D converter into the computer, digitally filtered to further remove non-dc components, and are then squared to yield the magnitude of the vector M^2. This vector is fully determined, as both Vr and C are defined internally (C from program tape, Vr from reference oscillator);

$$\therefore \boxed{M^2 = \left(\frac{VrC}{2}\right)^2}$$

The quantity M^2 is calculated in the computer, and from this point control proceeds in the identical manner as was described for the non-tracking operations.

It is not necessary to know the value of α as this drops out in the squaring process, whereas the product of the reference sine or cosine wave by the remaining harmonic terms average to zero contributions.

7.8 Generation of Shock Pulses and Shock Spectra

With the proper peripherals and software, the digital control system may be programmed to electronically synthesize a desired shock spectrum through the generation of simple, or complex shock pulses at the exciter table.* This becomes evident from inspection of the solution to the classical first-order damped system where the maximum relative response $\ddot{Z}(t)$ is given by:

$$Z(t) = -\frac{1}{\omega_d} \int_o^t \ddot{X}(\tau) e^{-\alpha\omega_n(t-\tau)} \sin \omega_d (t - \tau) d\tau$$

and

$$\ddot{Z}(t) = \left| Z(t) \cdot \omega_n \right|^2$$

where:

ω_n, ω_d = natural and damped frequencies, respectively,

α = percent critical damping,

**Typically achieved using series of damped sinusoids generated by fast Fourier transform techniques or voltage-control methods.*

$\ddot{X}(t)$ = input acceleration, and

$\ddot{Y}(t)$ = system acceleration

t = time

τ = integration variable

The capability to *electronically* shape the input acceleration-time history, using simple or complex waves, affirms the potential use of the DDC system as a simulator of a wide range of military shock-spectra environment. All that is required is the appropriate software package. An important feature of this software routine is its ability to automatically compute the shaker/load transfer function and correct the input pulse to achieve the desired spectra.

The versatility of the DDC system is, therefore, further enhanced by its potential utilization as a combined *vibration-and-shock* test control equipment. The system should be able to produce most simple shock pulses as specified in MIL-STD-810B and other Army applications. In most cases, however, the constraints on specific pulses are dictated more by the limitations of the test equipment than by the limitations of the electronics of the DDC system.

A thorough evaluation of the DDC system shock performance and capabilities is planned following the investigation of the DDC/random test system. Several manufacturers are supplying shock-spectra routines with their DDC test systems.

7.9 Computer Data Rate for Digital Control of Sine Testing

An extremely important concept in digital control of real time continuous process is the rate at which data must be processed. This includes synthesis of the control signal and waveform reconstruction of sampled data. Review of literature indicates that for a system with up to eight inputs and a maximum excitation frequency of 5000 Hz, the data rate for a sweep-sine test must be approximately 100 kHz for accurate reconstruction of the feedback signal (1-percent distortion error). Time must also be provided for all necessary calculations. The resulting requirements are too fast for present day mini-computers. However, acceptable performance can be achieved if the computer is operated at its free information rate, rather than the speed associated with the shaker/exciter drive signal(s). The functions necessary for control can easily be performed at the information rate, provided the high-frequency signal(s) is processed by the peripheral hardware. The peripheral hardware acts as a buffer system between the high-speed process at the exciter and low-speed process at the computer, thereby enabling the computer to become an efficient controller.

In sinusoidal testing, the drive signal is considered by the computer as a pair (or compound) of binary numbers representing amplitude and frequency. This signal is generated by a digital oscillator responding to these command numbers. Detectors placed upstream of the analog-to-digital converter slow down the rate of incoming data from the feedback signal, allowing the computer to sample the data at its own free rate. (However, the process rate at the shaker is not affected.)

Modern sample-data theory states that the sampling rate must be at least twice the maximum test frequency for accurate data reconstruction. However, since the amplitude control achieved here is based on a dc level proportional to amplitude—rather than on reconstruction of a sine waveform—the required data rate is substantially *below* twice the maximum frequency component. For this system, using single channel control of sweep-sine testing between 5 and 3000 Hz, the sampling rate is a constant 512 samples/sec, and may drop to as low as 64 samples/sec around 10- to 12-Hz test frequency when operating in the tracked mode. Typical sinusoidal waveform of the input and feedback signal, under digital control, can be easily identified from the illustrations presented with the test results in section 10.3.

To initiate an "abort" condition (when the test envelope is violated), a number of successive out-of-bound samples is required. These samples (data frames) are automatically optimized in the program to account for such parameters as sweep rate and test frequency. The range for this test system will vary between 8 and 32 successive data frames. Hence, the maximum time a test package could exceed or fall short of the test envelope is equal to 8/64 = 0.125 sec. For the typical heavy or medium force electro-dynamic exciters, the system reaction time to abort command could easily exceed this figure (i.e., reaction time could be 200-msec plus).

The count to initiate an "abort condition" is based on successive deviations. It is not cumulative, and will stall at zero if, for example, only 7 out-of-bound data frames are sensed.

7.10 Digital-Computer Word Format

In general, there are three possible word formats that could be used to represent a number. The first format can be called "fixed point." With this word format, the binary (or decimal) point is assumed to be at a specific location in the word and it does not change. For example:

BASE 10	BASE 2
3000.00	101110111000.0000000
0001.00	000000000001.0000000
$1 \le x \le 3000_{10}$	$1 \le x \le 3000_{10}$
6 DIGITS	19 DIGITS

A second possible word format can be called "floating point," or "scientific notation." In decimal form this format consists of the most significant portion of a number multiplied by ten to some integer power ($.X*10^N$). In a binary form, this word would be represented by the most significant portion of a number in binary format and the binary number so representative of two to some integer power ($.X2^N$). For example:

BASE 10	BASE 2
$.300*10^4$	$.1011101*2^{1100}$
$.999*10^0$	$.1111111*2^{0000}$
$X*10^N$	$X*2^N$
$.1_{10} \leq x \leq 1.0_{10}$	$.5_{10} \leq x \leq 1.0_{10}$
$0 \leq N \leq 4_{10}$	$0 \leq N \leq 15_{10}$
N = 0,1,2...	N = 0,1,2...
4 DIGITS	11 DIGITS

A third possible word format would be the binary number expressed as two to some power (2^N) where the power includes fractional quantities. This is called "logarithmic." In this third format, the most significant portion of the binary number is not directly apparent since the binary number is in log form. For example:

BASE 10	BASE 2
$10^{3.477}$	$2^{1011.101}$
10^{0000}	$2^{0000.000}$
10^N	2^N
$0 \leq N \leq 3.477_{10}$	$0 \leq N \leq 11.625_{10}$
4 DIGITS	7 DIGITS

A listing comparing the relative merits of each format is shown in the table III. This table shows the possible dynamic range for each format with the constraint that the binary number should be resolved to better than 1-percent accuracy. Since the dynamic range of the "fixed-point" approach is so limited, this method can be discarded immediately. The selection of the word format is then a choice of "floating point" or "log." The required word length for a specified dynamic range capability

TABLE III. DYNAMIC RANGE VERSUS FORMAT FOR NUMBER REPRESENTATION

Word length bits	Fixed point (dB)	Floating point (dB)	Logarithmic (dB)
17	60		
16	54		
15	48	768	
14	42	384	768
13	36	192	384
12	30	96	192
11	24	48	96

is a consideration in this choice. If a 96-dB dynamic range capability is acceptable, then the floating-point format can be used requiring 12 bits.

Use of the floating point as a data format instead of log is attractive. If we select the log format, a log conversion and anti-log conversion scheme is required to perform linear additions and subtractions. If this scheme is implemented directly in the computer, a great amount of time is required to do the translation.

With the floating-point format, additions can be made almost directly so that any averaging scheme is straightforward. Also, it is relatively simple for the computer to translate from binary floating point to decimal, so that input commands can be given in decimal with a fairly rapid translation into the binary-word format. If the most significant portion of the floating-point number is the number used in standardizing the transducer sensitivity, then the (2^N) of the number can be used for range changing in 6-dB steps.

8. DIGITALLY-CONTROLLED SWEEP SERVO OSCILLATOR

8.1 Technical Considerations(*)

The digitally-controlled sweep oscillator is a waveform synthesizer controlled by a floating-point digital number, which is generated by the digital computer. The digital computer transfers frequency, phase, and amplitude information to the oscillator via addressable registers located within the memory of the oscillator. Advantages realized through this approach to sine-vibration testing include: (a) automatic communication with a digital controller, (b) stability, (c) predictable distortion, and (d) instantaneous response to computer command.

In slaving the oscillator to a digital controller, the oscillator requirement for wide dynamic range, frequency resolution, and long-range stability must not be compromised. Otherwise, higher harmonic distortions, introduced during high-frequency testing, will tend to degrade the quality of measurement. The dynamic range of at least 60 dB must be maintained

---

**This section contains paragraphs from Reiner's report on Digitally-Controlled Sweep Servo Oscillator (see ref 2).*

to allow a step change of three orders of magnitudes (i.e., from 0.1 to 100 g). Also, the oscillator typically should have a wide-band frequency resolution of about 0.1 percent.

To meet the interface communication requirements of a digital controller as well as to permit adaptability to the "building-block" concept (where peripheral chassis can be added to existing system to expand its capability), a new generation of servo-oscillators had to be designed. The technically feasible solution for complying with the resolution requirements of the oscillator is based on the variable clock-oscillator technique. Frequency and waveform generation techniques had to be developed; also requiring development were techniques for floating-point commands for computer-controlled frequency sweep through sequential frequency command increments.

8.2 Oscillator Considerations

A sine-wave oscillator should typically conform to the following performance: (a) 1 to 10,000-Hz frequency band, (b) frequency resolution of 0.1 percent of point, (c) dynamic range of 60 dB minimum, (d) waveform distortion—50 dB below full scale, (e) phase resolution of -1 deg. Frequency programming is effected by reading a compound control word of modulus A and exponent N. This word consists of a total of 14 bits, bits 1 to 10 allocated for A, bits 11 to through 14 reserved for exponent N. To meet the low-distortion output waveform criteria, the number and location of the voltage steps must be determined. Modern sampled data theory predicts, provided quantizing errors are eliminated in a step size synthesis, the earliest harmonic frequency to be at the clocked rate. The theory proved to be correct in practice; it was found that a sine-wave synthesized from 128 clocked steps met the distortion requirements. Figure 7 displays the shape of a sine wave exactly as synthesized and also filtered by an rc pole approximately a decade away from the fundamental component.

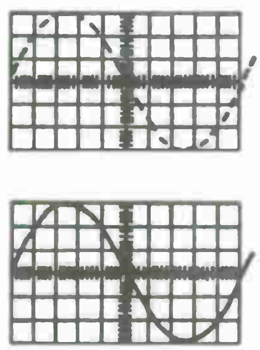


Figure 7. Sine wave synthesized from 128 clocked steps (32 polarity inverted steps).

Fine resolution between octave steps is obtained by varying the oscillator frequency by 2^{10} steps within any given octave. This is accomplished through the implementation of a digitally-controlled phase-lock loop, to precisely control the clock-oscillator frequency relative to a high-stable fixed-frequency reference oscillator. The phase-lock loop is commanded by the modulus A term, and the octave is commanded by exponent N. These are related according to equation (10):

$$f_{out} = KA2^N$$

where,

$$K = 1 \text{ Hz} \qquad (10)$$

$$A = 0.5 \text{ to } 1 \text{ in } 1024 \text{ steps}$$

$$N = 0 \text{ to } 14 \text{ in } 15 \text{ steps}$$

K is a factor that relates the clock frequency in steps/Hz to the output, whereas A is binary word of 10 bits and N is 4 bits. The waveform synthesizer included in figure 8 shows its relationship to the synthesized clock frequency f_2 where

$$f_{out} = f_2 \times M^{-1} \qquad (11)$$

$M \leq 512$ in binary steps.

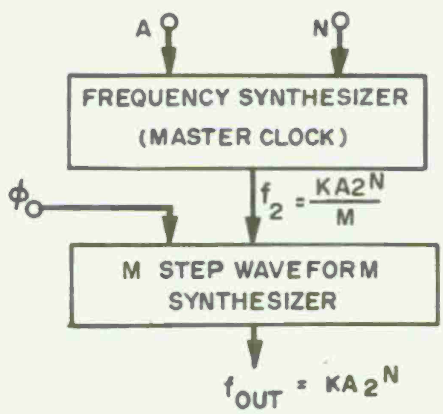


Figure 8. Waveform synthesizer.

In actual application, there are only 128 steps that comprise the synthesized waveform. However, that is reduced to only a quarter cycle, or 32 steps. In this way, the hardware necessary to implement the waveform can be minimized. The additional steps between 128 and 512 are provided for more precise phase-control capability but otherwise do not in any way contribute to waveform resolution.

8.3 Frequency-Synthesizer Section

The frequency-synthesizer section is shown in figure 9. The master or clock oscillator which forms the heart of the system is a voltage-controlled oscillator (VCO). It has a basic frequency range between 4 and 8 MHz which can be commanded by dc voltage. The 10-bit modulus A command word, supplied by the computer and stored in the (A) storage register essentially sets the VCO frequency. The value of A has a maximum 2:1 range in 1024 steps and is interpreted by the computer as having a modulus extending from .1111111111 to .1000000000, base 2 or approximately .999 to .5 in base 10. The binary number stored in storage register (A) provides VCO frequency control by means of a phase-lock loop.

The phase-lock loop maintains precise frequency control over the VCO, which becomes the master-clock oscillator for the system. A command word of modulus A is transferred to the (A) storage register when the strobeline to the (A) register is enabled. The storage

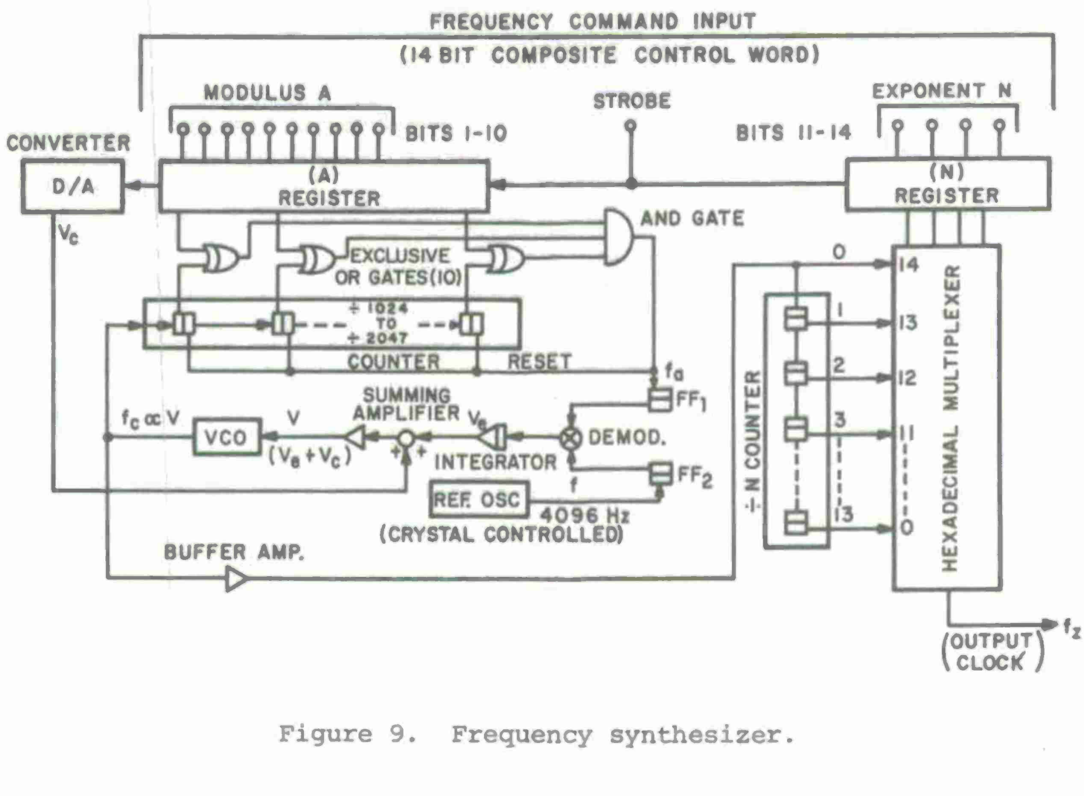


Figure 9. Frequency synthesizer.

register simultaneously supplies the binary information to a D/A, digital to analog, converter and also to 10 EXCLUSIVE-OR gates. The D/A converter supplies a preset command voltage through a summing amplifier to the input of the VCO. This voltage is used to initially preset the oscillator frequency to the vicinity of the final value desired. The output of the oscillator is applied to a counter composed of 10 JF flip-flops serially connected. The state of each of these flip-flops is interrogated by EXCLUSIVE-OR gates connected to each flip-flop output. As the counter counts the clock, which is the output of the VCO, the flip-flops count down until the state of the counter matches the state of the control lines in the (A) storage register. At that instant, the output of all the EXCLUSIVE-OR gates are simultaneously up or 1, producing an output pulse at the output of the AND gate which follows. The resulting AND gate output pulse serves two functions—it resets the counter so that the same counting sequency may repeat, and it drives FF1 (flip-flop 1), which is a trigger flip-flop. The T flip-flop output changes state at each trigger pulse to produce a square-wave output having a frequency related to the VCO frequency by exactly 2A where A is the modulus of the storage register (A). When the output of FF1 is compared with the output of FF2 in a demodulator, the demodulator output when integrated will have a dc level that varies as the phase angle between the two flip-flops supply square-wave signals. The dc voltage output from the demodulator, which is a voltage proportional to phase, is summed with the preset command voltage. The action of the phase loop is to provide a dc error correction voltage which, when summed with the preset command voltage, is applied to the VCO control input to command the precise frequency needed to lock the phase-lock loop. Then the output frequency from FF1 is nearly in quadrature with the output frequency of FF2. Similarly, when the command word is changed, a new preset command level is established and the control loop cycle repeats to achieve lock within 10 msec. The action of the loop is to always set the VCO frequency to whatever value is needed to maintain the output frequency from FF1 exactly equal to the frequency of FF2 (where FF2 is clocked from a reference oscillator). The output frequency from the VCO, therefore, always increases in direct proportion to the frequency division provided by the counter where the number of counts per cycle is commanded by storage register (A). It is clear that because the storage register (A) command has a capability of one step less than 2^{11} steps, the counter will be commanded to provide a clock-frequency division anywhere between 1024 and 2047. The VCO frequency will increase in exactly the same proportion. Any drift in VCO frequency due to such parameters as aging, temperature effects, set point drift will immediately result in a phase-angle change when compared with the reference oscillator phase. This produces a dc output level change proportional to phase-angle difference at the demodulator in a direction to correct the oscillator frequency toward a phase locked condition.

The output from the VCO is also supplied through a buffer amplifier as a clock frequency to a ÷ N, divide-by-N, counter. This counter is composed of (N-1) flip-flops.

Since N (max) for the oscillator is 14, only 13 flip-flops in series are needed to implement the frequency range desired. All flip-flops in the ÷ N counter have their output states connected to a multiplexer. The multiplexer can be considered a solid-state single-pole switch that responds to the address corresponding to the status word of the four binary-coded command lines supplied from the (N) storage register. When a number N between 0 and 14 is strobed into the storage register, a signal line is selected by the multiplexer corresponding to the number at the control input to the multiplexer. The multiplexer, then, makes the necessary connections between the ÷ N counter and the output, f_2. This multiplexing means also allows selection of any flip-flop sequency, allowing selection of a weighted complement of N to relate input command proportionally to output frequency.

The frequency f_2 from the frequency-synthesizer section is also directly related to f_{out} frequency of the oscillator by the number of independent steps needed by the waveform synthesizer, equation (2), to produce one complete cycle of sine-wave output.

8.4 Waveform-Synthesizer Section

The waveform synthesizer accepts the input clock frequency f_2, and follows the position of each clock pulse within a complete waveform cycle. In this way, specific voltage levels are assigned to clocked steps within the complete waveform cycle. Many repetitive waveforms can be synthesized by this method, as the independent steps are implemented by programmable resistive dividers. In this synthesizer, a complete output frequency cycle will be composed of 128 independent voltage steps. Then, in order to properly implement the phase-control resolution, the actual clock frequency is four times higher at 512 steps per output cycle. In this way, the phase resolution will be better than 1 deg.

Although 512 steps provide the desired phase resolution, the first four input pulses per step are ignored by the voltage-step synthesizer, thus relaxing the hardware requirement needed to produce the output waveform.

The waveform synthesizer section shown in figure 10 produces a sine wave with total harmonic distortion better than 40 dB below full-scale output. If a single-pole tracking filter is connected as shown, total harmonic distortion is reduced an additional 30 dB. A master counter tracks the position of each input clock pulse relative to the synthesized output frequency. If the output frequency is to be advanced in phase, a control word of modulus B is strobed into the phase register. Then, as the next output cycle begins, phase information is transferred to advance the associated flip-flops in the master counter. On the next clock pulse, further transfer is inhibited and uninterrupted counting proceeds. The absolute phase of the oscillator is always

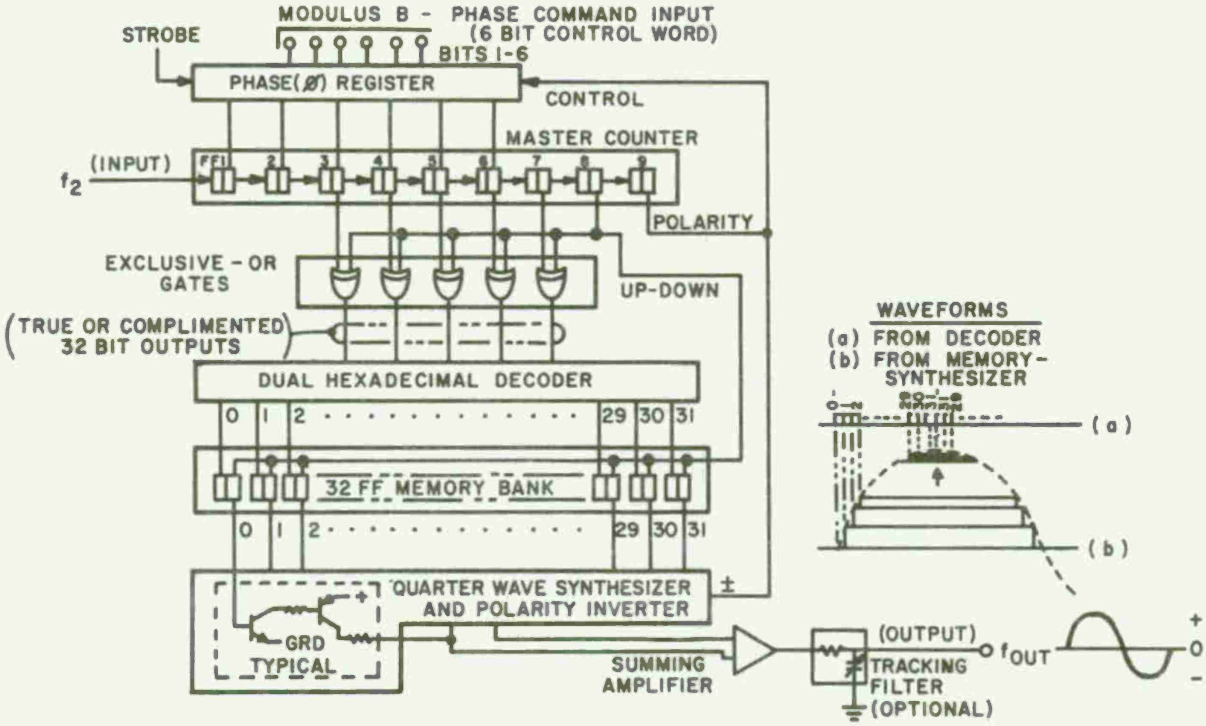


Figure 10. Waveform synthesizer.

available for computer interrogation by reading the state of the master counter at a time reference interval. The phase command can be repeated in increments of a few degrees per cycle or as a single-phase step correction. The proper phase angle is recognized by the computer when compared with the output of a second servo oscillator. Flip-flops 3 through 7 in the master counter supply discrete waveform step information, flip-flop 8 supplies up-down command, and flip-flop 9 supplies polarity command.

The reason for the up-down and polarity command lies with the fact that synthesis of only a quarter of a complete cycle is actually performed. Actually, only 32 of 128 discrete steps of frequency command are used to command the output-voltage levels. As the counter sequentially steps from 0 through 31, the synthesized output voltage rises from 0 to a positive maximum having a quarter sine-wave envelope. On the next clock pulse to flip-flop 3 of the master counter, flip-flops 3 through 7 go from state 1 to state 0, and flip-flop 8 changes state from 0 to 1, which is the countdown command.

The down command is applied to each of the five EXCLUSIVE-OR gates. These gates, with the down command enabled, invert the counter states flip-flops 3 through 7 and provide what is known as the complement of the binary number being supplied. As the flip-flops again count up from 0 through 31, the output of the EXCLUSIVE-OR gates under control of the down command count from 31 to 0. In this way the second quarter cycle of the output waveform is produced. Following this the

count-up command is again enabled. This would ultimately result in a full-wave rectified waveform except for the polarity command which commands opposite polarity voltage to that previously used to supply the voltage-divider steps in the quarter-wave synthesizer area. By this technique, a full cycle can be generated from a quarter cycle of analog information. (It is also possible to change the step-divider ratios and generate any other regular waveform that can be implemented on a quarter-cycle basis.)

Returning to the synthesizer circuit, the dual hexadecimal decoder accepts binary-coded information in either true or complemented form and accordingly enables one of 32 command lines. A memory bank of flip-flops driven from the command lines from the hexadecimal decoder synthesizes an output waveform pyramid of contiguous steps resulting in divider ratios developed through the progressive paralleling of incremental current steps. This technique has been found to be effective in reducing step-generated noise while contributing significantly to step accuracy. The result of this is to have a repeatably high quality synthesized waveform with controlled characteristics. In some instances of application, an optional tracking filter may be serially connected to the oscillator output. This filter is used to smooth the stepped wave into a waveform that is smooth and continuous. In the instance of the synthesized sine wave, the resulting filtered waveform seen in section 8.2 has the appearance of a sine wave generated from the more conventional analog oscillator circuit techniques.

8.5 Summary of Section 8

(1) The sweep-servo oscillator has wide dynamic range and high resolution. This is accomplished through use of a variable frequency master-clock oscillator controlled by a special purpose phase-lock loop. Conventional design techniques are used in the phase-lock loop design, although it is unusual in the digital method by which its output frequency is changed.

(2) The sine-wave output signal, constructed entirely of digital steps, has a very stable waveform characteristic over the entire operating range and has better than comparable distortion levels, compared with oscillators that produce synthesized sine-wave output through analog circuitry. Precise phase control between two oscillators is also readily provided by advancing either output signal in discrete incremental steps.

(3) All controlling commands are generated from a mini-computer, programmed to communicate commands to the oscillator in a combination of pure binary or floating point words.

(4) Spectrum analysis on the output sine wave has confirmed that the first significant harmonic distortion term is at the clock frequency, provided quantizing errors are eliminated in the waveform synthesis process. This is contrary to a misconception that third or fifth harmonic terms predominate.

(5) Inherent to the digital compatibility of the oscillator is the use of a variable frequency oscillator to produce an output frequency proportional to a binary input word of modulus A.* This is preferred over the conventional fixed-frequency clock oscillator.

III. <u>TEST RESULTS, TEST DATA, HIGH-LEVEL TESTS, AND STATE-OF-THE-ART DEVELOPMENTS FOR DDC OF DYNAMIC TESTING</u>

9. TESTS PERFORMED UNDER DIGITAL CONTROL

9.1 <u>Vibration-Test Matrix</u>

Twenty-three sine-sweep tests, as well as a mixed sine/random test, were selected based on specifications MIL-STD-810B, -331, and -167 for performance under direct-digital control (DDC). These tests practically cover the entire spectrum of the Army's field environment for such equipment as aircraft, helicopters, missiles, air/ground launch vehicles, fuzes, amphibious crafts, and transportation platforms. Successful execution of these tests by the DDC test system clearly attest to the viability of the digital control concept when applied to the stringent requirements of military dynamic testing. Furthermore, it also demonstrates the capability of the DDC test system to execute any other Army sine-sweep vibration test(s) in support of production/ qualification testing, limited only by the system or shaker electro-mechanical constraints.

All tests selected herein are listed in the test matrix (table IV). They comprise a representative sample group of maximum, nominal, and minimum field environment listed in the described specifications. Military standards 810B and 331 were selected because they comprise the standard requirements to which the bulk of the Army's field hardware must be qualified. Tests 21 through 24 in the matrix (table IV) were selected from MIL-STD-810C, which contains a proposed update for some of the vibration tests listed in 810B. Test No. 24 required a mixed operating mode whereby four separate sine waves coexist with a specified PSD spectra. This environment, which is based on field data for helicopter gun firing, was selected to simulate in the laboratory a complex field condition using the concept of direct-digital control. Although this DDC test system had demonstrated the capability to perform a mixed sine/random test during its acceptance test program, mixed testing was not possible as the software was being modified by the manufacturer. Test No. 24 will therefore be attempted as part of the random-test program scheduled next.

**This method will yield a frequency signal proportional to d-c level.*

TABLE IV. TEST MATRIX—DIRECT-DIGITAL CONTROL OF ARMY SWEEP-SINE VIBRATION TESTS

Test No.	Equipment Environmental Category	Test identification			
		Specification	Figure No.	Curve para	Resonance dwell frequency (Hz)
1	Airplanes/Helicopter (cat. a)	MIL-STD-810B (10-20-69)	514.1-1	Z	11.8
2	"		514-1-1	B	500.0
3	Airplanes (cat. b)		514.1-2	C	5.0
4	"		514.1-2	H	2000.0
5	"		514.1-2	L	100.0
6	Helicopter (cat. c)		514.1-3	M	33.0, 66.0
7	Air-Launch Missiles (cat. d)		514.1-4	C	250.0
8	"		514.1-4	H	22.5
9	"		514.1-4	AR	10.0
10	"		514.1-4	N	none
11	Ground Launch Missiles (cat. e)		514.1-5	P	none
12	"		514.1-5	U	none
13	Ground Vehicles		514.1-6	V	500.0
14	"		514.1-6	W	8.5
15	Transportation/Common Carrier, Land or Sea (cat. g)		514.1-7	AX	5.5
16	"		514.1-7	AV	28.0
17	Shipboard/Amphibious	MIL-STD-167	Type 1		7.5, 21.0, 42.0
18	Transportation Vibration (continuous method)	MIL-STD-331 (1-10-66)	Test 104	5.1.2.1	none
19	Transportation Vibration (Discrete method)	"	Test 104	5.2.1.1	11.0, 33.0, 59.0
20	Rough Handling (Continuous Method)	"	Test 114	5.2.1	21.0, 61.0
21	External Stores-Helicopters (Vertical)	MIL-STD-810C (proposed spec)	(see fig. 11)	A	5.0
22	Transverse	"	"	B	100.0
23	Longitudinal	"	"	C	33.0
24	Gunfire-Helicopter (Mixed Sinc/Random Test)	MIL-STD-810C (proposed spec)	"		none

SINUSOIDAL CYCLING TEST TIME

NUMBER OF MISSIONS	CYCLING TIME PER AXIS (MINUTES)
0-50	30
51-100	60
101 - ∞	90

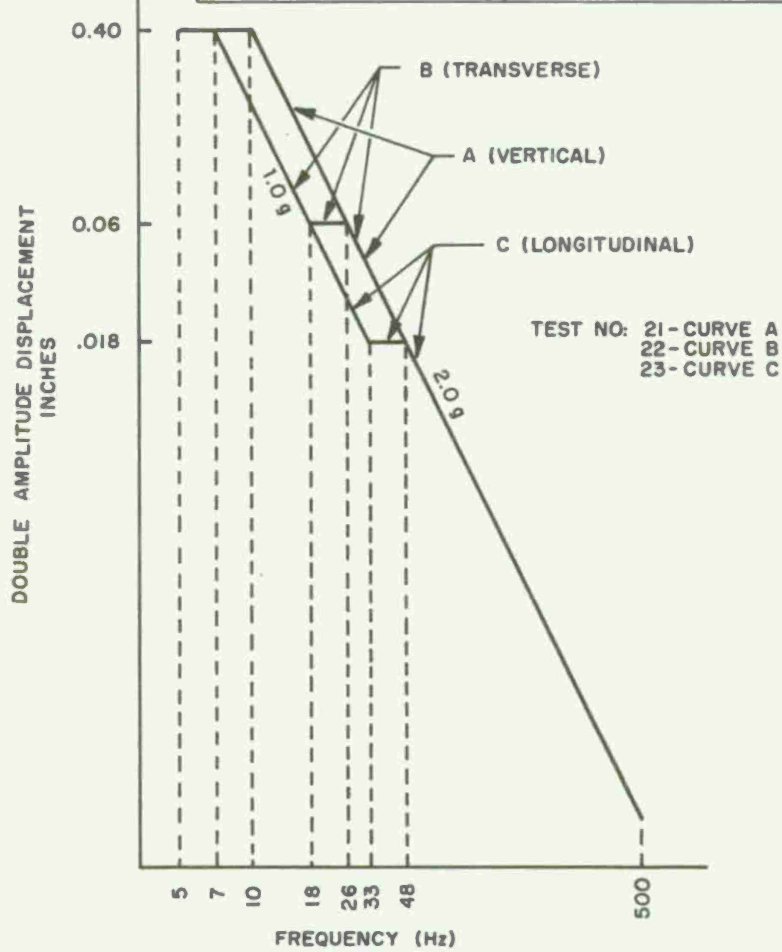
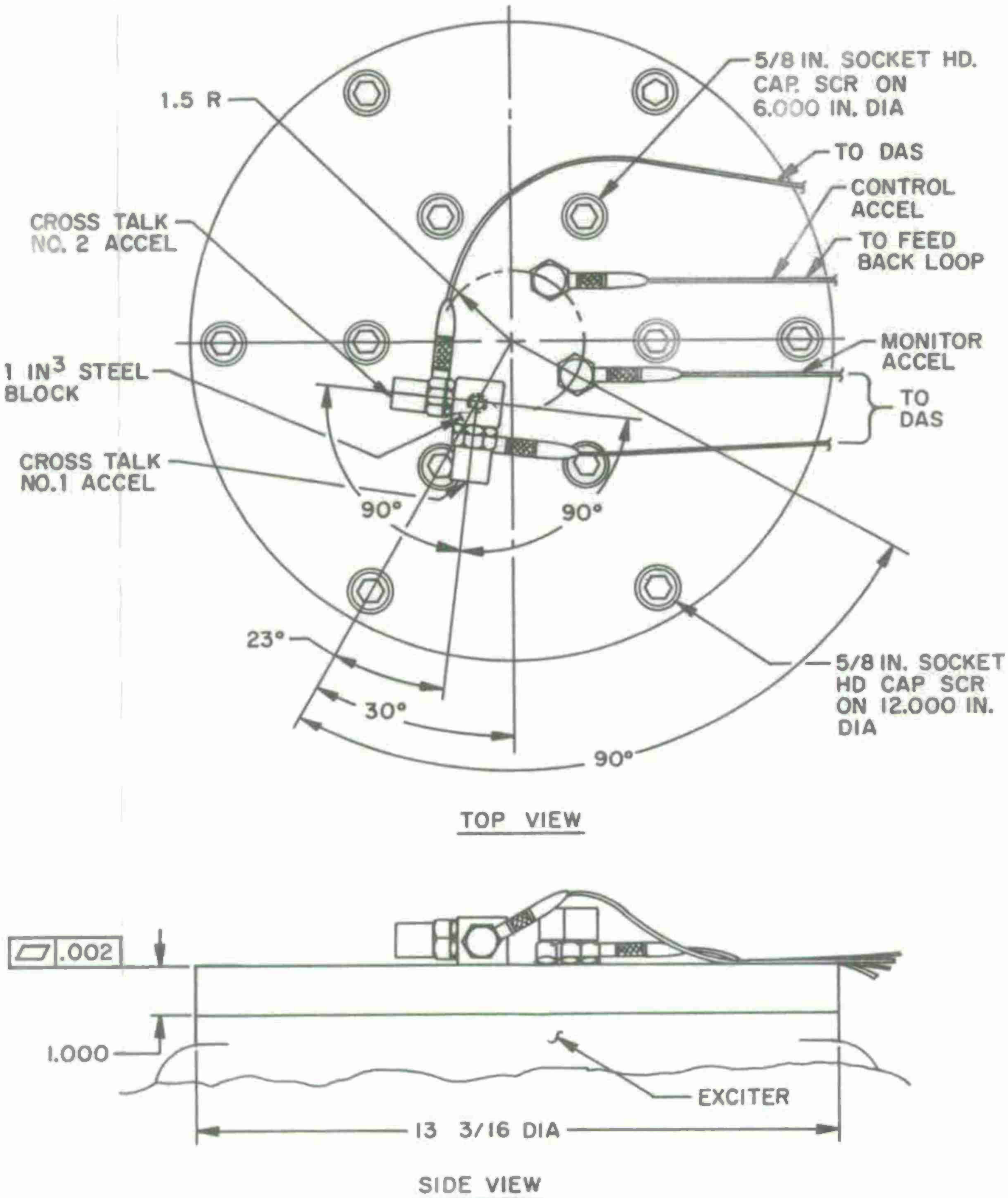


Figure 11. Vibration test curves for cycling test for externally carried stores for helicopters.
(Source: Proposed MIL-STD-810C, David L. Earls, Air Force Flight Dynamics Laboratory, WPAFB, Ohio.)

9.2 Test Fixture and Instrumentations

The test fixture consisted of a 13-3/16 in. o. d., 1.00-in.-thick aluminum (2024-T4) plate, fastened to the shaker table by six 5/8-in. bolts located on a 6.00-in. diameter and 12.00-in.-diameter bolt circle.

This plate was available from prior test work, and offered a convenient platform for accelerometer mounting. A detailed drawing of the test fixture and instrumentation is presented in figure 12; the test setup is presented in figure 13.



NOTES:

1. MIL-A-2550 APPLIES
2. MAT'L: ALUM ALLOY, PLATE, 2024 T4.
3. BOTH SIDES

Figure 12. Vibration test fixture and instrumentation for DDC evaluation.

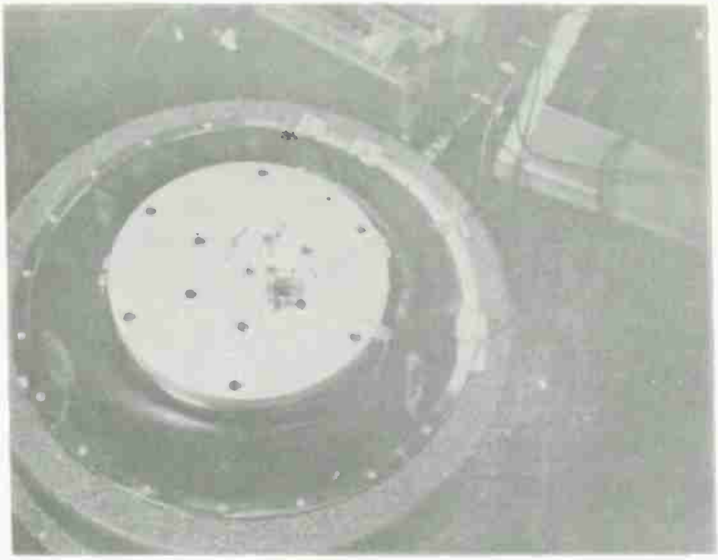


Figure 13. Top view photograph of shaker, test fixture (circular plate); control accelerometer; monitor accelerometer; and two block mounted cross-talk accelerometers.

The control accelerometer was connected to the feedback loop of the DDC test system. To independently confirm the voltage output of the control accelerometer, a monitor accelerometer was placed on the same diameter as the control accelerometer (3.00 in.) but 90 deg clockwise. Two additional accelerometers were mounted on a 1-in.^{3} steel block to verify that the in-plane (cross talk) vibrations complied with the test specifications. (The cross-talk measurements record vibrations in a plane perpendicular to the primary direction of motion; the allowable magnitude of the in-plane vibration must be $\leq$100 percent of the test level.) Orientation of the block was such that each cross-talk accelerometer sensed vibration vectors having radial and tangential components. Data from the two cross-talk accelerometers were acquired for selective tests only. The monitor accelerometer and the two cross-talk accelerometers provided data external to the DDC test system. These measurements were connected directly into the data acquisition system (DAS) via intermediate high-impedance Keithley isolation amplifiers. A detailed description of the DAS is presented in section 9.3.

All accelerometers were of the piezoelectric type manufactured by Endevco Corp. and were calibrated at 10 g against a standard accelerometer over the frequency range of 30 to 2000 Hz. The average sensitivity factor determined for each accelerometer is listed in table V.

TABLE V. AVERAGE SENSITIVITY FACTOR FOR TEST ACCELEROMETERS

Accelerometer	Model No.	Serial No.	Sensitivity factor $\left(\frac{mV\text{-}rms}{g}\right)$
Control	2233E	AJJ6	30.9
Monitor	2215C	LAD8	8.86
Cross Talk 2	2233	FE88	31.9
Cross Talk 1	2233	GA28	28.8
Cross Talk 2*[1]	2233E	AL59	32.1

(The four accelerometers were calibrated on April 1973 and possessed a valid calibration to April 1974. The calibration data are available but not included in this report.)

[1]*This cross-talk accelerometer No. 2 failed during test 13 and was replaced by cross-talk 2* accelerometer. The sensitivity of No. 2* accelerometer was computed from manufacturer data.*

9.3 Data Acquisition System (DAS)

A block diagram of the DAS used to externally monitor all test data is presented in figure 14. During low-level tests, for which the control accelerometer voltage output dropped below 10 mV, extraneous system noise resulted in frequent "alarm" message.* This condition was rectified by incorporating a scaling/charge amplifier into the feedback loop, which effectively raises the signal-to-noise ratio. The sensitivity of the control accelerometer was adjusted upward to 100 mV-pk/g from 42.7 mV-pk/g.

Commencing with test No. 4, the return signal from control accelerometer (isolated by the scaling/charge amplifier) was fed into the strip-chart recorder. Transducer output sensitivity was then set at 10 V full scale; this enabled the acquisition of analog voltage traces for both the monitor and control accelerometer while the two measurements were still synchronized in frequency and time.

An additional data record, semi-analog in nature, was available for the control accelerometer. This record consisted of a hard-copy plot of the digitized amplitude voltage versus test frequency and presented a log-log field. Frequency output is supplied by the signal-drive source, which is the digital oscillator, whereas amplitude information is provided by the A/D converter via the computer. Since the signal is not processed through a log converter here, the frequency response of this X-Y plotter is reliable down to 5 Hz, which is the lowest minimum test frequency. This plotter provides straight-line interpolation between any two discrete points, and cannot perform the plotting operation at the computer sample rate.

**An alarm message is printed out wherever the test amplitude exceeds the specified (±) control limit. The control limit for all tests was set at ±.92 dB (±10%).*

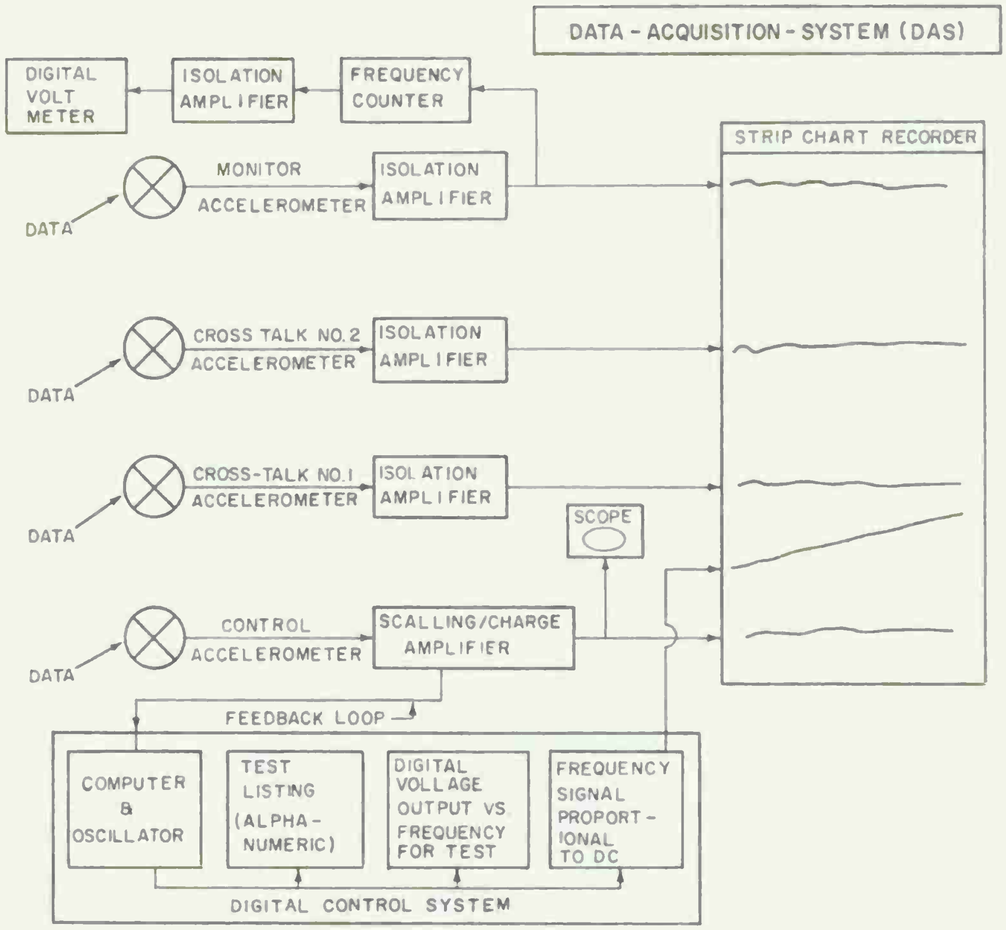


Figure 14. Block diagram of data acquisition system (DAS).

The configuration of the DAS was selected for the primary objective of demonstrating that the DDC test system, via the control accelerometer, will comply with the ±10-percent amplitude control requirement specified in MIL-STD-810B and 331. To achieve this, an independent confirmation of the control accelerometer data was required. The strip-chart recorder was adequate in collecting analog data during the sweep/dwell operation; but since each channel must be calibrated in discrete voltage steps, data for in-between steps had to be extrapolated—a process that introduces additional errors. In addition, the frequency response of the recorder was ±1.0 dB over the range of interest, clearly inadequate to measure errors of about ±1.0 dB. Therefore, a frequency counter and a digital voltmeter (DVM having a total error of <<.5 percent) were connected to the monitor accelerometer. The voltage output of this measurement was then recorded at each level of interest while the test was placed in the dwell mode. (It was impossible to ascertain accurate voltage data during the sweep operation as the

binary conversion circuits in the DVM are too slow to stabilize.) Also available was a digital printout of the test profile, which discretely listed the arithmetic time average of the test amplitude at each 1/3 octave points, as executed by the control accelerometer. This configuration made possible a reliable comparison between the monitor and control accelerometers.

9.4 Instrumentation Description

The isolation amplifiers connected to the external accelerometers (through 185 PF cable) were Keithley Instruments model 102B, operating on X1 scale ratio. Specifically these were:

For monitor accelerometer: K. A. Serial No. 20858 (HDL - D021383); calibration not required.

For cross-talk 1 accelerometer: K. A. serial No. 20252 (HDL - D021384); Valid calibration to April 1974.

For cross-talk 2 accelerometer: K. A. serial No. 12385 (HDL LJ574); calibration not required.

For frequency counter and DVM: K. A. serial No. 22380 (HDL D022690); calibration not required.

The remaining instruments consisted of:

Frequency counter: General Radio 1191-B
dc, 20-MHz frequency range
40-dB max attenuation;
valid calibration (June-Dec 1973).

Digital voltmeter: Dana Digital Multivoltmeter Model 5800
100 dB of noise attenuation at 60 Hz for both signal and reference voltage; ac frequency down to 10 Hz.

Maximum error—.14 percent reading +.02 percent of full scale; valid calibration Sept 1973-Apr 1974.

Strip-Chart Recorder: Gould Brush Recorder model 200,
10 to 100 kHz ± 1-dB frequency response
(-3 dB at 7 Hz).

Linearity/accuracy 0.5 dB over 50-dB range.

Average a-c sensing; calibration not required (HDL 34104).

Scaling/charge amplifier: Endevco Charge Amplifier model 2730;
Under valid calibration (see calibration sect below).

Calibration. — Each channel of the strip-chart recorder was calibrated before each test. Using a Ballantine true rms voltmeter (HDL 24891 calibrated to 9 Oct 1973), a 10-level-per-channel calibration was performed using a 1-kHz (rms) input signal. Full scale typically consisted of 10 mV (rms) or 300 mV (rms) for the external accelerometers, and 10 V for the control accelerometer. The four Keithley amplifiers were then calibrated at their X1-, X10-, X100-scale magnification. A 10-mV (rms) signal at 1 kHz was fed into each amplifier from the Ballantine voltmeter, and then displayed on a digital voltmeter which indicated 10, 100, and 1000 mV for the respective magnification scales, thereby completing the calibration process.

Frequency calibration of the strip-chart recorder was performed as per figure 15 (one channel only).

9.5 DDC Test System—Electromechanical Limits

Force, displacement, and power constraints impose electromechanical limitations on the performance of the electrodynamic exciter and the test system. When operating in the sine-sweep mode, the exciter's displacement velocity, and acceleration/force can be determined from the classical simple harmonic motion. By applying the foregoing procedure, the operator can insure that the preprogrammed safety limits of the test system are not violated; this will further reduce setup time by eliminating erroneous program inputs. Let the acceleration ($\ddot{X}$) be subjected to harmonic excitation of amplitude (g) and driving frequency (w) so that

$$\ddot{X} = g \sin wt \tag{12}$$

and

$$(\ddot{X})\ \max = |g| \tag{13}$$

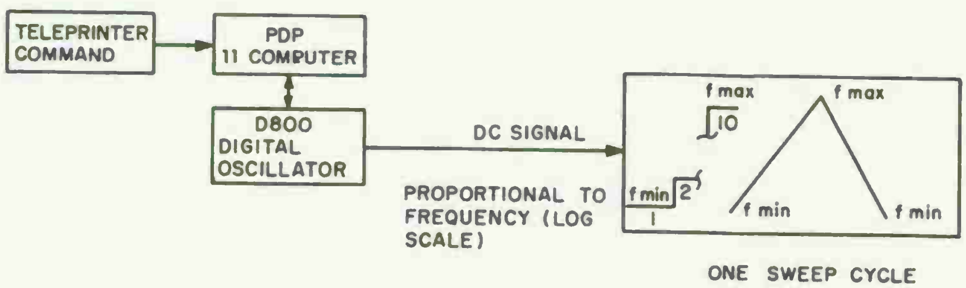


Figure 15. Frequency calibration setup.

The resulting maximum velocity ($\dot{X}$) and displacement (X) are determined by successive integrations of equation (12).

$$\dot{X} = \int^t \ddot{X}\, dt = \frac{-g}{w} \cos wt$$

$$(\dot{X}) \max = \left|\frac{g}{w}\right| , \tag{14}$$

and

$$X = \int^t \dot{X}\, dt = \frac{-g}{w^2} \sin wt$$

$$(X) \max = \frac{g}{w^2} . \tag{15}$$

The maximum acceleration, velocity, and displacement as a function of input acceleration and driving frequency are defined by equations (13), (14), and (15), respectively. Conversely, the resulting maximum acceleration at a specific frequency and known displacement for velocity can also be ascertained. Once these parameters are determined, bearing in mind that the mass of the test package is known, it is simple to insure that any specified test envelope will comply with the electromechanical limitations of the test system. The DDC test system contains an interval software routine that automatically checks every test entry against all allowable limits. Any entry that exceeds these preprogrammed limits will preclude the punchout of the data tape, a status that does not permit testing. Erroneous entries cause the printout of informing the operator of the limit(s) violated. The T5021 system is limited to 120 g over the frequency range of 5 to 3000 Hz when operating in the sine mode. The maximum velocity and displacement expressed in engineering units are:

$$\text{Let } (XW) \leq g = 120\ g\ (g = 386\ \text{in./sec}^2),$$

$$g \geq \frac{\dot{x}(\text{in./sec})\ w(\text{cyc/sec})\ x\ 2\pi\ \text{rad/cyc}}{386\ \text{in./sec}^2} = 1.63 \times 10^{-2}\ (X\omega) \sim g\text{'s}.$$

And

$$(\dot{X})\ \max \leqq \frac{120}{1.63 \times 10^{-2}\ w} \cong \frac{7362}{w} \sim \text{in./sec.} \qquad (16)$$

Where $w \geqq$ lowest frequency at which the maximum limit of the displacement (X) is violated.

Also let $(XW^2) \leq g = 120\ g$

$$g \geq \frac{X(\text{in.})\ (W\ \text{cyc/sec} \times 2\pi\text{rad/cyc})^2}{2 \times 386\ \text{in./sec}}$$

$$g \geq 5.10 \times 10^{-2}\ (XW^2) \sim \text{in g's.} \qquad (17)$$

And

$$(X)\ \max < \frac{120}{5.1 \times 10^{-2}}\ (W^2) = \frac{2353}{w^2} \sim \text{in.} \qquad (18)$$

where $W >$ lowest test frequency at which the maximum limit of the displacement (X) is violated. Note that equations (16) and (18) must be satisfied simultaneously.

The mechanical limitations of the T5021 system/C90 shaker, after applying the proper factors of safety, are given in table VI.

Attention must also be directed to the feedback signal so that it does not saturate the signal-conditioning unit(s). The accelerometer sensitivity must be of such that the maximum voltage output at any test level does not exceed the full range of the signal-conditioning unit. This is verified by multiplying the maximum (equivalent acceleration level defined in equations (15) and (17) by the sensitivity of the accelerometer.

Hence, $V_{out} \leq SX(g)\ \max$,

where

V_{out} = max. voltage range of signal condition unit (= 5.0 V for this system)

S = Transducer sensitivity,* $\frac{\text{mV-pk}}{g}$, or mV-rms/g

$(g)\ \max$ = maximum test acceleration level

**As defined in software.*

TABLE VI. T5021 SYSTEM/C90 SHAKER LIMITS

Parameters	Minimum	Maximum	Units
Displacement	4.49×10^{-6}	0.75	in. (D.A.)
Velocity	1×10^{-3}	50.0	in./sec
Acceleration	5×10^{-2}	120.0	g's
Force	(2.0)	7000.0	lb
Frequency (oscil only)	0.5	16,000	Hz
Frequency actual (this system)	5	3000.0 (sine)	"
	5	5000 (random)	"
Sensitivity	1.0	1000.0	mV pk/g
ALARM/ABORT	±0.5	±50.0	dB

10. Test Data Analysis

Sections 10.1 through 10.6 contain a detailed analysis of the data obtained for all tests specified in the test matrix (table IV). Also presented are selected analog and digital data records for comparison and demonstration purposes. Each test was performed in accordance with the applicable requirements specified in MIL-STD-810B, -331, -167, and -810C. Test data contained in subsequent sections demonstrate that the DDC test system can meet vibration performance levels well in excess of those required in the aforementioned specifications. Finally, the current state-of-the-art digital control techniques, as well as future developments as they apply to military dynamic testing are discussed.

10.1 Amplitude-Control Accuracy

Specifications in MIL-STD-810B and -331 require that the displacement or acceleration test amplitude be controlled to within ±10 percent of the specified value over the range of 5 to 2000 Hz. In fact, this requirement is typical of most military sine-sweep vibration tests. The test data were thoroughly analyzed at all frequencies and amplitudes (see tables VII through XXVII) to demonstrate compliance with this requirement. The results indicate that the DDC test system can easily satisfy this amplitude-control requirement. Deviations in the test

amplitudes, as determined by comparing data from the control accelerometer against data from the independent monitor accelerometer, were centered around +(5 ± 1) percent over the frequency range of 10 to 2000 Hz. No independent confirmation was possible in the 5-to 10-Hz frequency range as the digital voltmeter (a highly accurate instrument used to record data for the monitor accelerometer) was limited to 10 Hz. Confirmation of amplitude control accuracy for the 5-to 10-Hz band was obtained through analysis of amplitude voltage plots presented in figures 16 through 37. These figures portray the frequency spectra of the amplitude voltage information as digitized by the A/D converter. Application of the voltage sensitivity (mV/g) of the transducer to these data permits direct conversion into displacement or acceleration amplitudes. Review of this processed data indicates the average deviation from the specified test amplitude to center around ±3.5 percent for the 5-to 10-Hz band.

Initially, excessive noise was encountered at the low-frequency range (5 to 15 Hz), resulting in intermittent loss of control outside the ±10-percent band. This loss of control occurred when the sensitivity of the control accelerometer was 42.7 mV-pk/g, and when the test amplitude was at a fraction of a g, for which the accelerometer voltage output fell below 10 mV. The incorporation of a scaling/charge amplifier, beginning with test No. 3, practically eliminated this problem by raising the transducer sensitivity to 100 mV pk/g. The remedy became evident when low-g tests were satisfactorily repeated at the low-frequency range with the increased transducer sensitivity. Amplitude ABORT and ALARM control limits were programmed at ±3.0 dB and ±.92 dB (±10 percent, respectively, for every test. Consequently, when test amplitude deviations exceeded the ±10-percent control requirement at any frequency (consecutively for the frequency dependent 8-32 data frames at 512-Hz sample rate), an ALARM message would be printed out by the computer. Review of all computer printouts for the increased transducer sensitivity indicated practically no ALARM messages at the 5- to 15-Hz band. The few ALARM messages detected were quite random in nature, and had a tendency to occur toward the very end of the test, a trend that might be attributed to electronic heating of the equipment.

The increased transducer sensitivity, however, cannot eliminate low-frequency waveform distortion associated with the dynamics of the shaker. Aside from extraneous noise, this is probably the major contributor to loss of control; or, in this case, to any inconsistencies that might develop between the two accelerometers at low frequencies. The DDC test system is controlling the test amplitude while tracking the frequency. This insures control to the absolute test sweep frequency, and eliminates all other harmonic contributions. On the other hand the monitor accelerometer records wide-band data, for which the test amplitude is made up of the fundamental frequency as well as all existing harmonic components. Photographs of the feedback signal confirm such a distortion trend for this shaker/specimen combination in the 5 to 33 Hz band (see sect 10.3.3).

TABLE VII. TEST NO. 1—TEST DATA ERROR EVALUATION

Date: 27 Sept 1973

(Test identification: MIL-STD-810B; figure 514.1-1; curve Z)

Frequency (Hz)	Ref test level at freq*	Digital rms voltage - monitor accel (mV)	Vibration test mode		% error	
			Monitor accel	Control accel	Control versus monitor**	Control versus ref***
10	.100 DA	5.2	.1148 DA	.1010 DA	-12.0	+1.0
15	.100	10.5	.1030 DA	.1010 DA	-1.94	+1.0
19	.100	10.5	.1009 DA	.1010 DA	+.10	+1.0
21	2.0 A	18.0	2.0310 A	2.000 A	-1.53	0.0
25	2.0 A	17.8	2.0090 A	2.000 A	-.45	0.0
29	2.0	17.7	1.9977 A	2.0005 A	+.14	+.25
34	.036 DA	18.5	.0353 DA	.0360 DA	+1.98	0.0
50	.036 DA	40.0	.0353 DA	.0360 DA	+1.98	0.0
68	.036 DA	74.5	.0356 DA	.0360 DA	+1.12	0.0
200	10.0 A	87.2	9.8420 A	9.970 A	+1.30	-.30
300	10.0 A	87.1	9.8307 A	9.980 A	+1.52	-.20
500	10.0 A	85.4	9.6388 A	10.000 A	+3.75	0.0

*DA = Displacement double amplitude (in.); A = acceleration (g)
**Defined in equation (12)
***Defined in equation (13)

TABLE VIII. TEST NO. 2—TEST DATA ERROR EVAULATION

Date: 27 Sept 1973

(Test identification: MIL-STD-810B; figure 514.1-1; curve B)

Frequency (Hz)	Ref test level at freq*	Digital rms voltage - monitor accel (mV)	Vibration test mode		% error	
			Monitor accel	Control accel	Control versus monitor**	Control versus ref***
9	.100 DA	4.03	.1098 DA	.1010 DA	-8.01	+1.0
13	.100 DA	7.63	.0096 DA	.1000 DA	+.40	0.0
17	.100 DA	12.30	.0939 DA	.1008 DA	+.73	+.80
20	2.00 DA	16.90	1.9074 A	2.0100 A	+5.38	+.50
120	2.00 DA	16.92	1.9097 A	2.0000 A	+4.73	0.0
290	2.00 DA	17.03	1.9221 A	2.0000 A	+4.05	0.0
360	2.00 DA	17.00	1.9187 A	2.0000 A	+4.24	0.0
480	2.00 DA	16.91	1.9085 A	2.0000 A	+4.79	0.0
500	2.00 DA	16.99	1.9176 A	2.0000 A	+4.30	0.0

*DA = Displacement double amplitude (in.); A = acceleration (g)
**Defined in equation (12)
***Defined in equation (13)

TABLE IX. TEST NO. 3—TEST DATA ERROR EVALUATION

Date: 27 Sept 1973

(Test identification: MIL-STD-810B; figure 514.2; curve C)

Frequency (Hz)	Ref test level at freq*	Digital rms voltage - monitor accel (mV)	Vibration test mode		% error	
			Monitor accel	Control accel	Control versus monitor**	Control versus ref***
8	.100 DA	-	-	.1010 DA	-	+1.0
11	.100 DA	6.5	.1186 DA	.1005 DA	-15.26	+0.5
14	.100 DA	8.7	.0911 DA	.1000 DA	+9.77	0.0
17	1.00 A	8.8	.9932 DA	1.0100 A	+1.69	+1.0
20	1.00 A	8.8	.9932 DA	1.0000 A	+.68	0.0
23	1.00 A	8.7	.9849 DA	1.0000 A	+1.84	+.3
32	.0360 DA	15.8	.0341 DA	.0361 DA	+5.54	0.0
41	.0360 DA	26.3	.0345 DA	.0360 DA	+4.35	0.0
50	.0360 DA	38.5	.0340 DA	.0360 DA	+5.88	0
164	5.00 A	42.3	4.7740 A	4.9800 A	+4.32	-.4
286	5.00 A	42.2	4.7630 A	4.9900 A	+4.16	-.2
396	5.00 A	41.8	4.7178 A	4.9800 A	+5.56	-.1
498	5.00 A	41.8	4.7178 A	4.9800 A	+5.56	-.4

*DA = Displacement double amplitude (in.); A = acceleration (g)
**Defined in equation (12)
***Defined in equation (13)

TABLE X. TEST NO. 4—TEST DATA ERROR EVALUATION

Date: 27 Sept 1973

(Test identification: MIL-STD-810B; figure 514.1-2; curve H)

Frequency (Hz)	Ref test level at freq*	Digital rms voltage - monitor accel (mV)	Vibration test mode		% error	
			Monitor accel	Control accel	Control versus monitor**	Control versus ref***
8	.100 DA	-	-	.1030 DA	-	+3.0
11	.100 DA	5.5	.1003 DA	.1040 DA	+3.70	+4.0
14	.100 DA	8.7	.0980 DA	.1040 DA	+6.1	+4.0
18	1.000 A	8.7	.9819 A	1.0000 A	+1.8	0.0
23	1.000 A	8.9	1.0045 A	1.0000	-.44	0.0
36	.0360 DA	20.0	.0341 DA	.0360 DA	+5.6	0
49	.0360 DA	37.0	.0340 DA	.0359 DA	+5.6	-.30
62	.0360 DA	59.2	.0340 DA	.0362 DA	+6.5	+.50
74	.0360 DA	84.8	.0342 DA	.0359 DA	+5.0	-.30
500	10.0 A	83.3	9.4018 A	9.9706 A	+6.0	-.30
1000	10.0 A	86.5	9.7630 A	9.970 A	+2.1	-.30
1500	10.0 A	89.5	10.1016 A	9.970 A	+1.3	-.30

*DA = Displacement double amplitude (in.); A = acceleration (g)
**Defined in equation (12)
***Defined in equation (13)

TABLE XI. TEST NO. 5—TEST DATA ERROR EVALUATION

Date: 27 Sept 1973

(Test identification: MIL-STD-810B; figure 514.1-2; curve L)

Frequency (Hz)	Ref test level at freq*	Digital rms voltage - monitor accel (mV)	Vibration test mode		% error	
			Monitor accel	Control accel	Control versus monitor**	Control versus ref***
11	.100 DA	6.2	.1131 DA	.101 DA	-10.7	+1.0
14	.100 DA	9.1	.1025 DA	.100	-2.4	0.0
17	1.00 A	8.8	.9932 A	1.0000 A	+.70	0.0
20	1.00 A	8.9	1.0045 A	1.0000	+.4	0.0
23	1.00 A	8.8	.9932 A	.998	+.5	-.20
43	.0360 DA	28.9	.0345 DA	.0359 DA	+4.0	-.30
63	.0360 DA	61.7	.0343 DA	.0359 DA	+4.7	-.30
104	.0360 DA	167.8	.0342 DA	.0359 DA	+5.0	-.30
500	20.0 A	168.7	19.040 A	20.0000 A	+5.0	0.0
1000	20.0 A	172.3	19.4469 A	19.9000 A	+2.3	-.5
1500	20.0 A	178.2	20.1129 A	19.9500 A	-.80	-.25
2000	20.0 A	184.2	20.790 A	20.0000 A	-1.30	0.0

*DA = Displacement double amplitude (in.); A = acceleration (g)
**Defined in equation (12)
***Defined in equation (13)

TABLE XII. TEST NO. 6—TEST DATA ERROR EVALUATION

Date: 27 Sept 1973

(Test identification: MIL-STD-810B; figure 514.1-3; curve M)

Frequency (Hz)	Ref test level at freq*	Digital rms voltage - monitor accel (mV)	Vibration test mode		% error	
			Monitor accel	Control accel	Control versus monitor**	Control versus ref***
11	.100 DA	5.7	.1040 DA	.1005 DA	-3.40	+.50
14	.100 DA	8.9	.1002 DA	.1005	+.30	+.50
23	2.0 A	17.1	1.9300 A	2.0100 A	+4.1	+.50
26	2.0 A	17.2	1.9413 A	2.0105 A	+3.6	+.52
29	2.0 A	17.2	1.9413 A	2.0105 A	+3.6	+.52
125	5.0 A	42.7	4.8194 A	4.9500 A	+2.7	-1.0
250	5.0 A	42.9	4.8420 A	4.9800 A	+2.8	-.40
375	5.0 A	42.8	4.8307 A	4.9890 A	+3.8	-.20
500	5.0 A	42.7	4.8194 A	4.9800 A	+3.3	-.40

*DA = Displacement double amplitude (in.); A = acceleration (g)
**Defined in equation (12)
***Defined in equation (13)

TABLE XIII. TEST No. 7—TEST DATA ERROR EVALUATION

Date: 27 Sept 1973

(Test identification: MIL-STD-810B; figure 514.1-4; curve C)

Frequency (Hz)	Ref test level at freq*	Digital rms voltage - monitor accel (mV)	Vibration test mode		% error	
			Monitor accel	Control accel	Control versus monitor**	Control versus ref***
11	.100 DA	5.5	.1003 DA	.1000 DA	+5.7	+6.0
14	.100 DA	8.8	.09912 DA	.100 DA	-.90	0
23	1.00 A	8.9	1.0045 A	.9980 A	-.60	-.2
26	.036 DA	11.1	.0362 DA	.0359 DA	-.8	-.3
29	.036 DA	13.5	.0354 DA	.0359 DA	+1.0	-.3
125	5.0 A	42.9	4.8420 A	4.9800 A	+2.8	-.4
250	5.0 A	42.9	4.8420 A	4.9700 A	+2.6	-.6
375	5.0 A	42.6	4.8081 A	4.9850 A	+3.6	-.3
500	5.0 A	42.5	4.7968 A	5.0000 A	+4.2	0.0

*DA = Displacement double amplitude (in.); A = acceleration (g)
**Defined in equation (12)
***Defined in equation (13)

TABLE XIV. TEST No. 8—TEST DATA ERROR EVALUATION

Date: 27 Sept 1973

(Test identification: MIL-STD-810B; figure 514.1-4; curve H)

Frequency (Hz)	Ref test level at freq*	Digital rms voltage - monitor accel (mV)	Vibration test mode		% error	
			Monitor accel	Control accel	Control versus monitor**	Control versus ref***
11	.1 DA	6.1	.1112 DA	.101 DA	-9.25	1
14	.1	8.9	.1002	.101	.75	1
17	1 A	8.9	1.0046	1 A	-.45	0
20	1 A	8.9	1.004	1 A	-.45	0
23	1 A	8.8	.99	1 A	.68	0
45	.036 DA	31.5	.0343 DA	.036 DA	4.8	0
57	.036	50.2	.0341	.03505 DA	2.75	-2.63
70	.036	75.7	.0341	.0358 DA	4.96	-.55
500	10 A	84.4	9.52 A	10 A	4.97	
1000	10 A	86.5	9.76 A	9.97 A	2.12	.30
1500	10 A	89.7	10.12 A	9.97 A	-1.52	
2000	10 A	92.2	10.41 A	10 A	-3.90	.30

*DA = Displacement double amplitude (in.); A = acceleration (g)
**Defined in equation (12)
***Defined in equation (13)

TABLE XV. TEST NO. 9—TEST DATA ERROR EVALUATION

Date: 27 Sept 1973

(Test identification: MIL-STD-810B; curve AR; figure 514.1-4)

Frequency (Hz)	Ref test level at freq*	Digital rms voltage - monitor accel (mV)	Vibration test mode		% error	
			Monitor accel	Control accel	Control versus monitor**	Control versus ref***
13	.1 DA	8.1	.1058 DA	.101 DA	-4.54	1
17	.1 DA	13.2	.1008 DA	.1015 DA	.65	1.5
20	.1 DA	17.9	.0987 DA	.1 DA	1.22	0
500	2 A	17.8	2.009 A	2 A	-.45	0
1000	2 A	17.9	2.020 A	2 A	-1.0	0
1500	2 A	18.5	2.088 A	2 A	-4.21	0
2000	2 A	18.9	2.1331 A	2 A	-6.24	0

*DA = Displacement double amplitude (in.); A = acceleration (g)
**Defined in equation (12)
***Defined in equation (13)

TABLE XVI. TEST NO. 10—TEST DATA ERROR EVALUATION

Date: 27 Sept 1973

(Test identification: MIL-STD-810B; curve N; figure 514.1-4)

Frequency (Hz)	Ref test level at freq*	Digital rms voltage - monitor accel (mV)	Vibration test mode		% error	
			Monitor accel	Control accel	Control versus monitor**	Control versus ref***
10	.2 DA	8.7	.192 DA	.201 DA	4.64	.5
12	1 A	8.9	1.004 A	1 A	-.45	0
15 1	1 A	8.7	.981 A	1.005	2.34	.49
18	1 A	8.8	.993 A	1	.68	0
20	.06 DA	9.8	.054 DA	.0601 DA	8.45	.16
24	.06 DA	14.4	.055 DA	.0601	8.89	.16
26	.06 DA	16.8	.054 DA	.0598	8.99	.33
500	2 DA	16.7	1.884 A	2 A	6.10	0
1000	2 DA	16.7	1.884 A	2 A	6.10	0
1500	2 DA	17.6	1.986 A	2 A	.68	0
2000	2 DA	17.6	1.986 A	2 A	.68	0

*DA = Displacement double amplitude (in.); A = acceleration (g)
**Defined in equation (12)
***Defined in equation (13)

TABLE XVII. TEST NO. 11—TEST DATA ERROR EVALUATION

Date: 27 Sept 1973

(Test identification: MIL-STD-810B; curve P; figure 514.1-5)

Frequency (Hz)	Ref test level at freq*	Digital rms voltage - monitor accel (mV)	Vibration test mode		% error	
			Monitor accel	Control accel	Control versus monitor**	Control versus ref***
10	.2 DA	8.5	.187 DA	.201 DA	7.11	.5
18	1 g	8.6	.97 g	1 g	3.02	0
24	.06 DA	14.8	.0567 DA	.0599 DA	5.59	-.16
30	.06	22.6	.0554 DA	.0604 DA	8.95	.66
35	.06	30.4	.0547 DA	.0601 DA	9.69	-.16
40	.06	39.6	.0546 DA	.0597 DA	9.25	-.49
500	5 A	40.9	4.61 A	4.98 A	7.87	-.4
1500	5	43.6	4.92 A	4.98 A	1.19	-.4
2000	5	44.8	4.97 A	5.00 A	.45	0

*DA = Displacement double amplitude (in.); A = acceleration (g)
**Defined in equation (12)
***Defined in equation (13)

TABLE XVIII. TEST NO. 12—TEST DATA ERROR EVALUATION

Date: 27 Sept 1973

(Test identification: MIL-STD-810B; curve U; figure 514.1-5)

Frequency (Hz)	Ref test level at freq*	Digital rms voltage - monitor accel (mV)	Vibration test mode		% error	
			Monitor accel	Control accel	Control versus monitor**	Control versus ref***
10	.2 DA	8.7	.192 DA	.201 DA	4.65	.5
15	1 A	9.1	1.027 g	1 A	-2.63	0
18	1	8.8	.993	1	.68	0
28	.06 DA	19.9	.056 DA	.0603 DA	7.6	.5
46	.06	53.5	.056 DA	.0599	7.3	-.167
74	.06	138.6	.056 DA	.06	7.3	0
102	.06	262.1	.056 DA	.0598	7.5	-.333
128	.06	448.4	.0604 DA	.0601	-.53	.167
157	50 A	448	50.56 A	50 A	-1.1	0
430	50	442.3	49.92 A	49.8	-.24	-.4
1000	50	451.9	51.00 A	49.7	-2.55	-.6
1500	50	465	52.48 A	49.8	-5.11	-.4
2000	50	472.2	53.29 A	49.9	-6.37	-.2

*DA = Displacement double amplitude (in.); A = acceleration (g)
**Defined in equation (12)
***Defined in equation (13)

TABLE XIX. TEST NO. 13—TEST DATA ERROR EVALUATION

Date: 27 Sept 1973

(Test identification: MIL-STD-810B; curve V; figure 514.1-6)

Frequency (Hz)	Ref test level at freq*	Digital rms voltage - monitor accel (mV)	Vibration test mode		% error	
			Monitor accel	Control accel	Control versus monitor**	Control versus ref***
10	1.5 A	12.3	1.38 A	1.5 A	8.04	0
50	1.5	12.8	1.44	1.5	3.8	0
100	1.5	12.8	1.44	1.49	3.1	-.67
200	1.5	12.8	1.44	1.5	3.8	0
300	1.5	12.9	1.46	1.49	2.3	-.67
400	1.5	12.7	1.43	1.49	3.9	-.67
500	1.5	12.7	1.43	.5	4.6	0

*DA = Displacement double amplitude (in.); A = acceleration (g)
**Defined in equation (12)
***Defined in equation (13)

TABLE XX. TEST NO. 14—TEST DATA ERROR EVALUATION

Date: 27 Sept 1973

(Test identification: MIL-STD-810B; curve W; figure 514.1-6)

Frequency (Hz)	Ref test level at freq*	Digital rms voltage - monitor accel (mV)	Vibration test mode		% error	
			Monitor accel	Control accel	Control versus monitor**	Control versus ref***
5	.75 DA			.723 DA		3.6
7	.75			.758		1.0
9	.75			.752		.26
12	3.5 g	21.9	2.47 A†	3.52 A		.57
15	3.5	21.7	2.45 †	3.52		.57
.8	3.5	21.8	2.46 †	3.52		.57
120	4 g	34.6	3.90 A	3.98 A	1.91	-.5
250	4	34.5	3.89	3.99	2.47	-.25
370	4	34.6	3.90	3.99	2.17	-.25
500	4	34.8	3.93	4	.8	0

*DA = Displacement double amplitude (in.); A = acceleration (g)
**Defined in equation (12)
***Defined in equation (13)
†Questionable data

TABLE XXI. TEST NO. 15—TEST DATA ERROR EVALUATION

Date: 27 Sept 1973

(Test identification: MIL-STD-810B; curve AX; figure 514.1-7)

Frequency (Hz)	Ref test level at freq*	Digital rms voltage - monitor accel (mV)	Vibration test mode		% error	
			Monitor accel	Control accel	Control versus monitor**	Control versus ref***
5	.75 DA			.777 DA		-3.6
7	.75			.76		.33
15	2 A	17.9	2.02 A	2.12 A	4.93	5.99
22	2	17.6	1.98	2.105	5.96	5.24
29	2	17.8	2.01	2.11	5.02	5.49
38	2	17.9	2.02	2.09	3.44	4.49
40	.036 DA	25	.0344 DA	.036 DA	4.36	0
42	.036	27.1	.0346	.036	3.84	0
120	3.5 A	30.1	3.40 A	3.48 A	2.43	-.51
240	3.5	30.2	3.41	3.495	2.53	-.14
360	3.5	30.2	3.41	3.49	2.39	-.28
480	3.5	29.6	3.37	3.48	3.11	-.57

*DA = Displacement double amplitude (in.); A = acceleration (g)
**Defined in equation (12)
***Defined in equation (13)

TABLE XXII. TEST NO. 16—TEST DATA ERROR EVALUATION

Date: 27 Sept 1973

(Test identification: MIL-STD-810B; curve AV; figure 514.1-7)

Frequency (Hz)	Ref test level at freq*	Digital rms voltage - monitor accel (mV)	Vibration test mode		% error	
			Monitor accel	Control accel	Control versus monitor**	Control versus ref***
6	.75 DA			.75		0
7	.75			.758		1.06
8	.75			.756		.8
16	1.5	13.5	1.52	1.51 A	.89	.67
24	1.5	13.3	1.50	1.505	.25	.33
32	1.5	13.3	1.50	1.52	1.26	1.33
39	.02 DA	13.5	.0195	.02 DA	2.06	0
42	.02	15.7	.0196	.02	1.78	0
45	.02	17.8	.0194	.0205	5.63	2.5
48	.02	20.3	.0194	.0201	2.33	.5
50	.02	22.2	.0196	.0201	2.52	.5
115	2.5 A	21.3	2.404 A	2.485 A	3.36	-.6
230	2.5	21.3	2.404	2.487	3.44	-.52
345	2.5	21.4	2.415	2.485	2.88	-.6
460	2.5	21.5	2.426	2.49	2.61	-.4

*DA = Displacement double amplitude (in.); A = acceleration (g)
**Defined in equation (12)
***Defined in equation (13)

TABLE XXIII. TEST NO. 17—TEST DATA ERROR EVALUATION

Date: 27 Sept 1973

(Test identification: MIL-STD-167B; equipment type I)

Frequency (Hz)	Ref test level at freq*	Digital rms voltage - monitor accel (mV)	Vibration test mode		% error	
			Monitor accel	Control accel	Control versus monitor**	Control versus ref***
4	.03 DA	N	.0345 DA	.0292 DA		-2.7
8	.03	O	.0302	.02999		-.03
.5	.03	T	.0307	.02994		-.2
.7	.02		.0200	.0198		-1
20	.02		.0200	.02		0
25	.02	A	.0207	.01995		-.2
27	.01	V	.0100	.0099		-1.0
30	.01	A	.0104	.0096		-.4
33	.01	I	.0104	.009985		-.2
35	.005	L	.0054	.00502		.4
40	.005	A	.0053	.00499		-.2
42	.003	B	.0031	.002975		-.8
46	.003	L	.0028	.0029825		-.6
50	.003	E	.0032	.002995		-.2
			Analog Data	Digital Data		

*DA = Displacment double amplitude (in.); A = acceleration (g)
**Defined in equation (12)
***Defined in equation (13)

TABLE XXIV. TEST NO. 18,19—TEST DATA ERROR EVALUATION

Date: 27 Sept 1973

(Test identification: Test 104, MIL-STD-331) [18-20 Hz→60 Hz: 19-60 Hz→500 Hz]

Frequency (Hz)	Ref test level at freq*	Digital rms voltage - monitor accel (mV)	Vibration test mode		% error	
			Monitor accel	Control accel	Control versus monitor**	Control versus ref***
20	2 A	16.3	1.83 A	2 A	8.71	0
30	2	16.4	1.85	2.01	8.59	.49
40	2	16.5	1.86	2	7.39	0
60	2	16.5	1.86	2	7.39	0
60	5 A	41.2	4.65 A	4.89 A	5.15	-2.2
147	5	41.7	4.70	4.98	5.81	-.4
294	5	41.8	4.71	5	5.98	0
441	5	41.3	4.66	4.99	7.04	-.2

*DA = Displacement double amplitude (in.); A = acceleration (g)
**Defined in equation (12)
***Defined in equation (13)

TABLE XXV. TEST NO. 20—TEST DATA ERROR EVALUATION

Date: 27 Sept 1973

(Test identification: procedure 114, MIL-STD-331)

Frequency (Hz)	Ref test level at freq*	Digital rms voltage - monitor accel (mV)	Vibration test mode		% error	
			Monitor accel	Control accel	Control versus monitor**	Control versus ref***
15	.09 DA	8.6	.084 DA	.0906 DA	7.36	.67
20	.09	14.8	.082	.0898	9.93	-.22
21	.06 DA	11.5	.057 DA	.0601 DA	4.39	.167
30	.06	22.8	.056	.0601	7.45	.167
40	.06	40.4	.056	.0601	7.81	.167
50	.06	63.2	.056	.0601	7.68	.167
60	.06	91.6	.056	.0605	7.70	.83
61	10 A	81.9	9.24 A	9.97 A	7.85	-.3
190	10	83.2	9.39	9.99	6.38	-.1
320	10	83	9.37	9.97	6.42	-.3
450	10	82.2	9.28	9.97	7.46	-.3

*DA = Displacement double amplitude (in.); A = acceleration (g)
**Defined in equation (12)
***Defined in equation (13)

TABLE XXVI. TEST NO. 21—TEST DATA ERROR EVALUATION

Date: 27 Sept 1973

[Test identification: MIL-STD-810C (Proposed); curve A]

Frequency (Hz)	Ref test level at freq*	Digital rms voltage - monitor accel (mV)	Vibration test mode		% error	
			Monitor accel	Control accel	Control versus monitor**	Control versus ref***
10	.4 DA	16.6	.36 DA	.4 DA	9.1	0
170	2 A	16.8	1.89 A	2 A	5.48	0
340	2 A	16.8	1.89 A	2 A	5.48	0
500	2 A	16.5	1.86 A	2 A	7.39	0

*DA = Displacement double amplitude (in.); A = acceleration (g)
**Defined in equation (12)
***Defined in equation (13)

TABLE XXVII. TEST NO. 22—TEST DATA ERROR EVALUATION

Date: 27 Sept 1973

(Test identification: MIL-STD-810C (Proposed); curve b)

Frequency (Hz)	Ref test level at freq*	Digital rms voltage - monitor accel (mV)	Vibration test mode		% error	
			Monitor accel	Control accel	Control versus monitor**	Control versus ref***
20	.06 DA	10.2	.056 DA	.0599 DA	.22	.33
26	.06 DA	16.8	.054	.0601	9.53	.167
31	.06 DA	24.1	.055	.0602	8.75	.33
32	.06 DA	25.7	.055	.0603	8.82	.49
155	2 A	16.8	1.89 A	2 A	5.47	0
310	2 A	16.8	1.89	2 A	5.47	0
460	2 A	16.6	1.87	2 A	6.74	0

*DA = Displacement double amplitude (in.); A = acceleration (g)
**Defined in equation (12)
***Defined in equation (13)

TABLE XXVIII. TEST NO. 23—TEST DATA ERROR EVALUATION

Date: 27 Sept 1973

[Test identification: MIL-STD-810C (Proposed); curve C]

Frequency (Hz)	Ref test level at freq*	Digital rms voltage - monitor accel (mV)	Vibration test mode		% error	
			Monitor accel	Control accel	Control versus monitor**	Control versus ref***
7	.4 DA			.409 DA		2.25
15	1 A	8.6	.97 A	1.0 A	3.00	0
23	1 A	8.5	.96	.999	4.10	.1
32	1 A	8.5	.96	1.01	5.27	.999
40	.018 DA	12.3	.0169 DA	.0181 DA	6.64	.555
48	.018 DA	17.5	.0167	.0181	7.94	.555
150	2 A	16.7	1.88 A	2.005 A	6.37	.25
300	2 A	16.8	1.89	2	5.47	0
450	2 A	16.6	1.87	2	6.7	0

*DA = Displacement double amplitude (in.); A = acceleration (g)
**Defined in equation (12)
***Defined in equation (13)

Test No: 1 Date: 9-27-73 Figure 16
Test ID: MIL-STD-810B

Figure: 514.1-1 Curve: Z

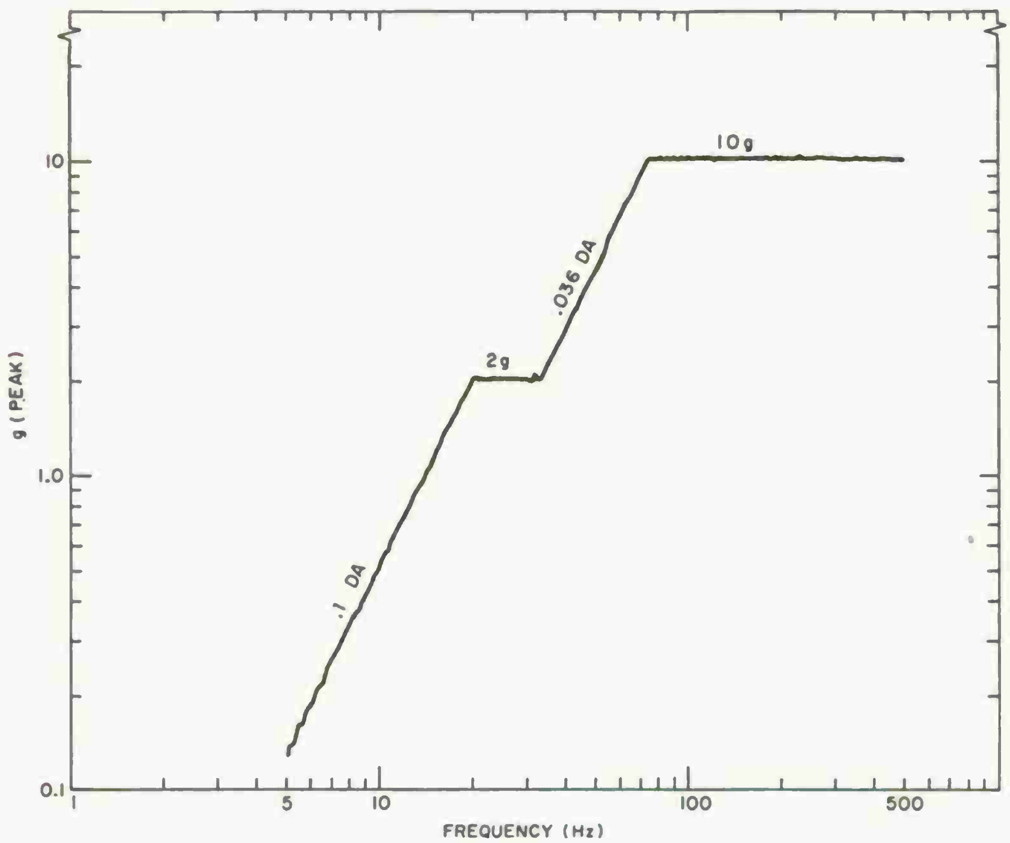


Figure 16. Equivalent digitized amplitude voltage versus sweep frequency.

(all curves were "traced from original data.")

Test No: 2 Date: 10-1-73 Figure 17
MIL-STD-810B

Figure: 514.1-1 Curve: B

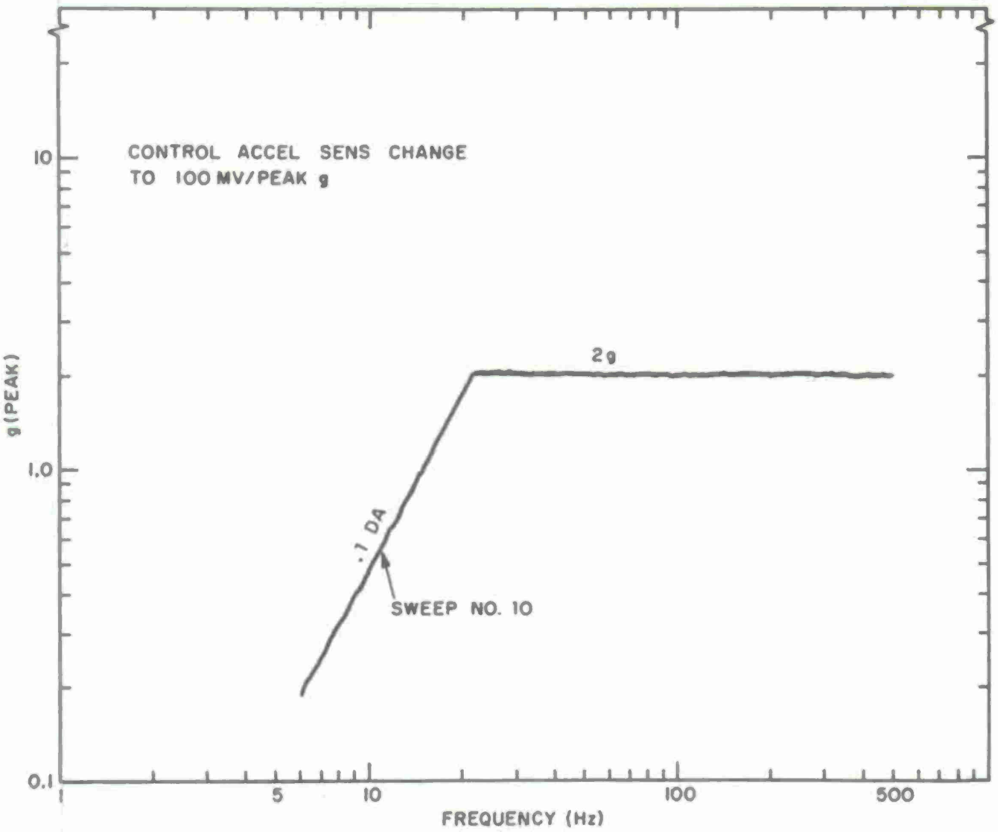


Figure 17. Amplitude voltage plot for test No. 2.
(all curves were "traced from original data.")

Test No: 3
Test ID: MIL-STD-810B

Figure 18

Figure: 514.1-2 Curve: C

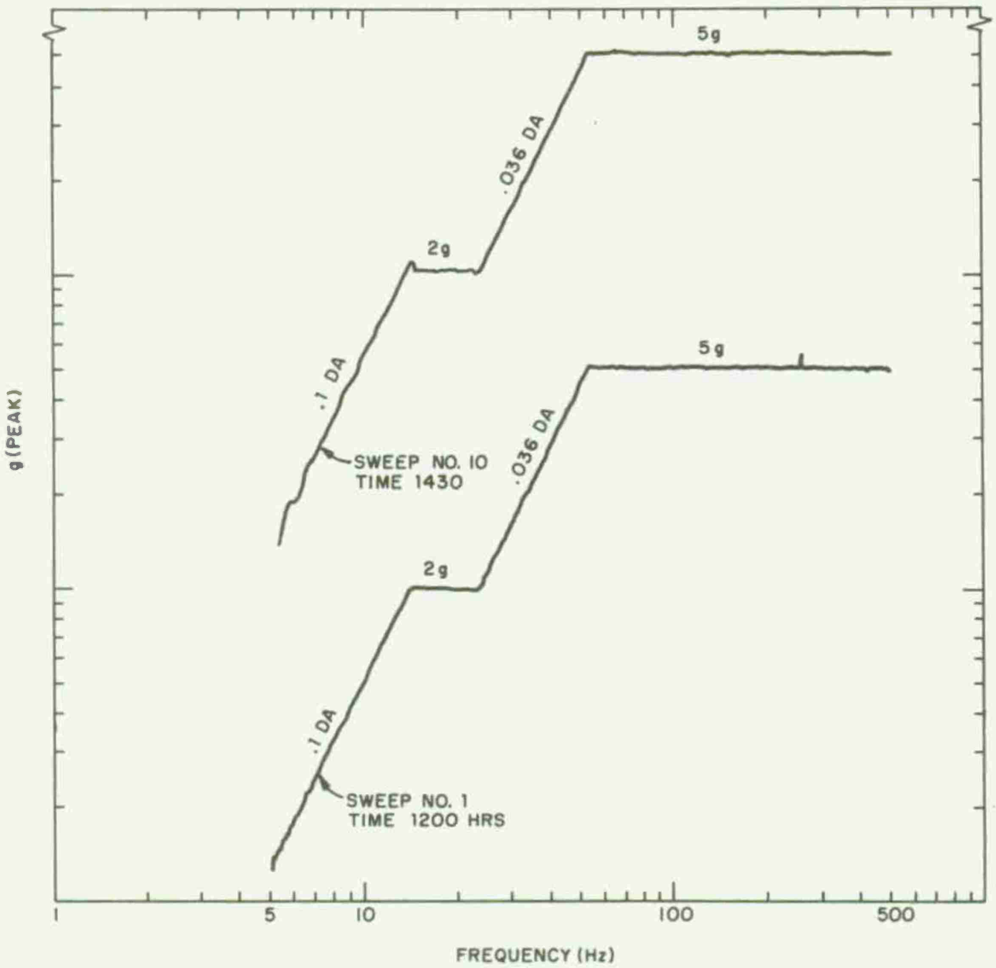


Figure 18. Amplitude voltage plot for test No. 3.

(all curves were "traced from original data.")

Test No: 4 Date: 10-2-73 Figure 19
MIL-STD-810B

Figure: 514.1-2 Curve: H

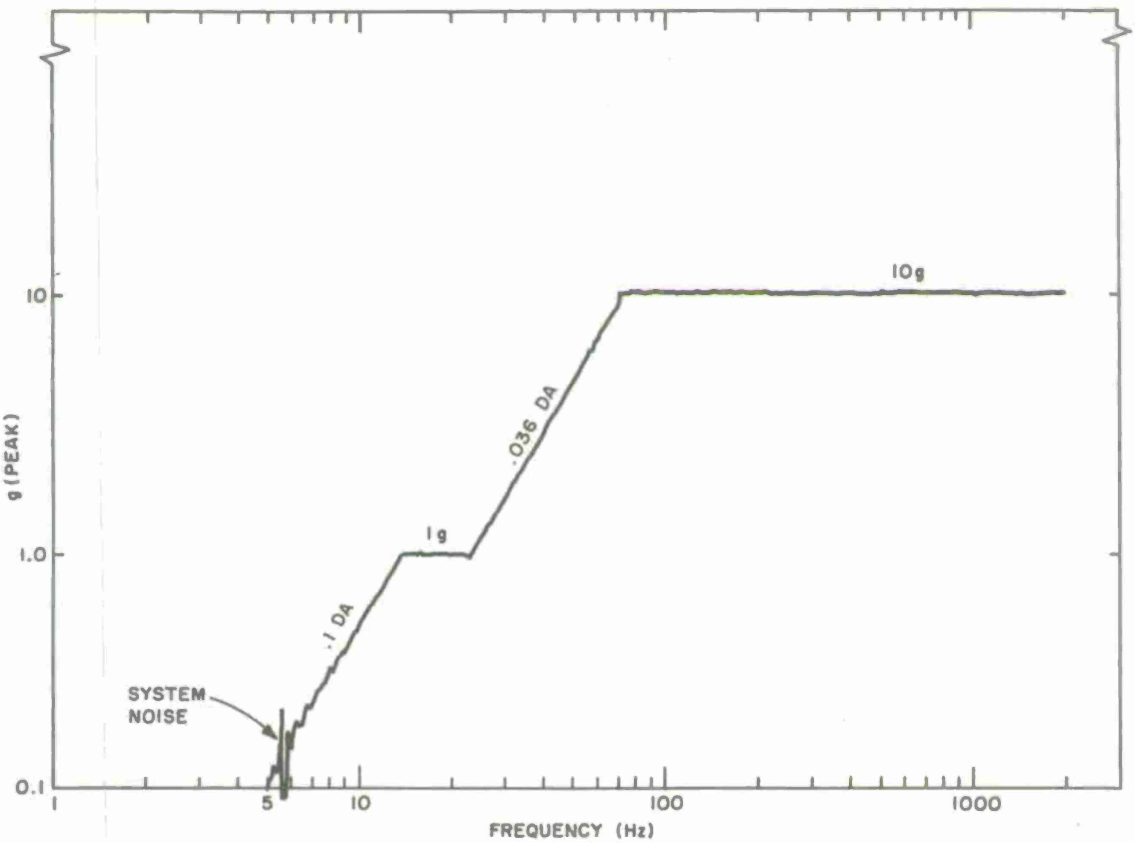


Figure 19. Amplitude voltage plot for test No. 4.

(all curves were "traced from original data.")

Test No: 5 Date: 10-4-73 Figure 20
Test ID: MIL-STD-810B
Figure: 514.1-2 Curve: L

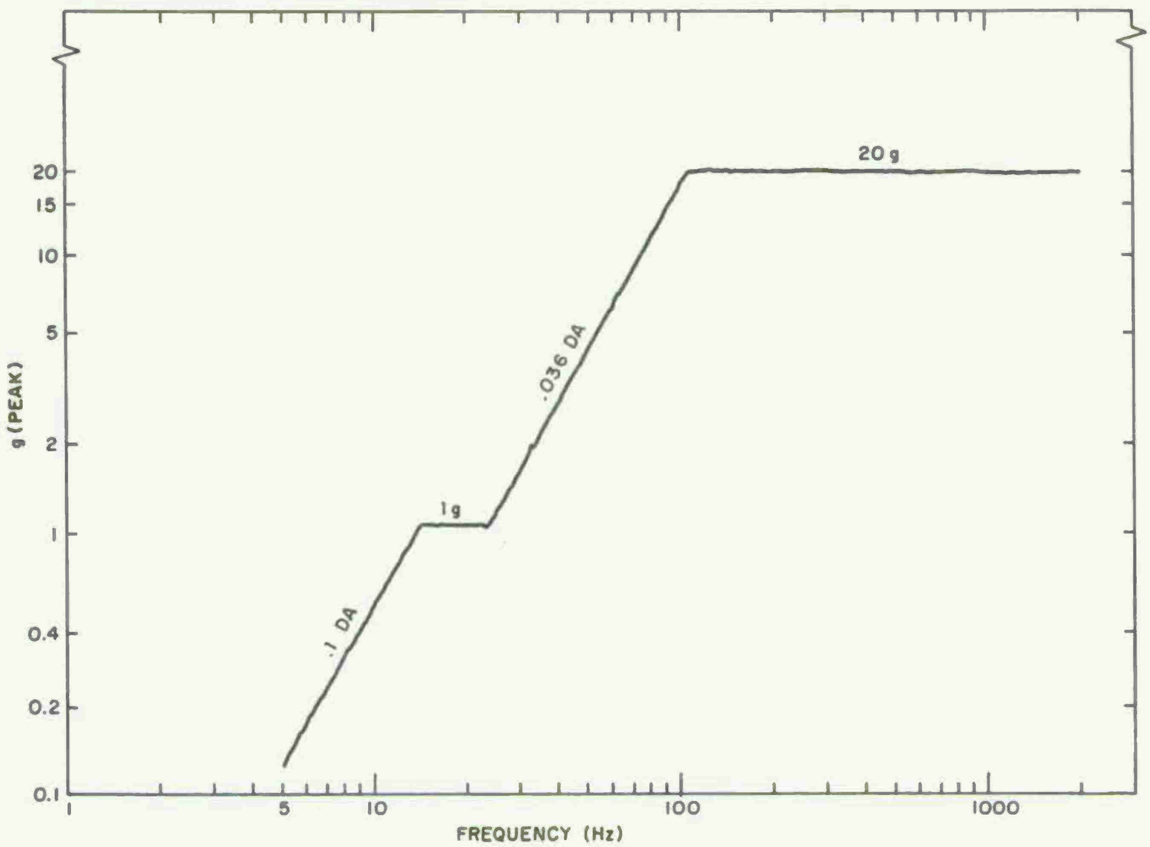


Figure 20. Amplitude voltage plot for test No. 5.
(all curves were "traced from original data.")

Test No: 6 Date: 10-4-73 Figure 21
Test ID: MIL-STD-810B

Figure: 514.1-3 Curve: M

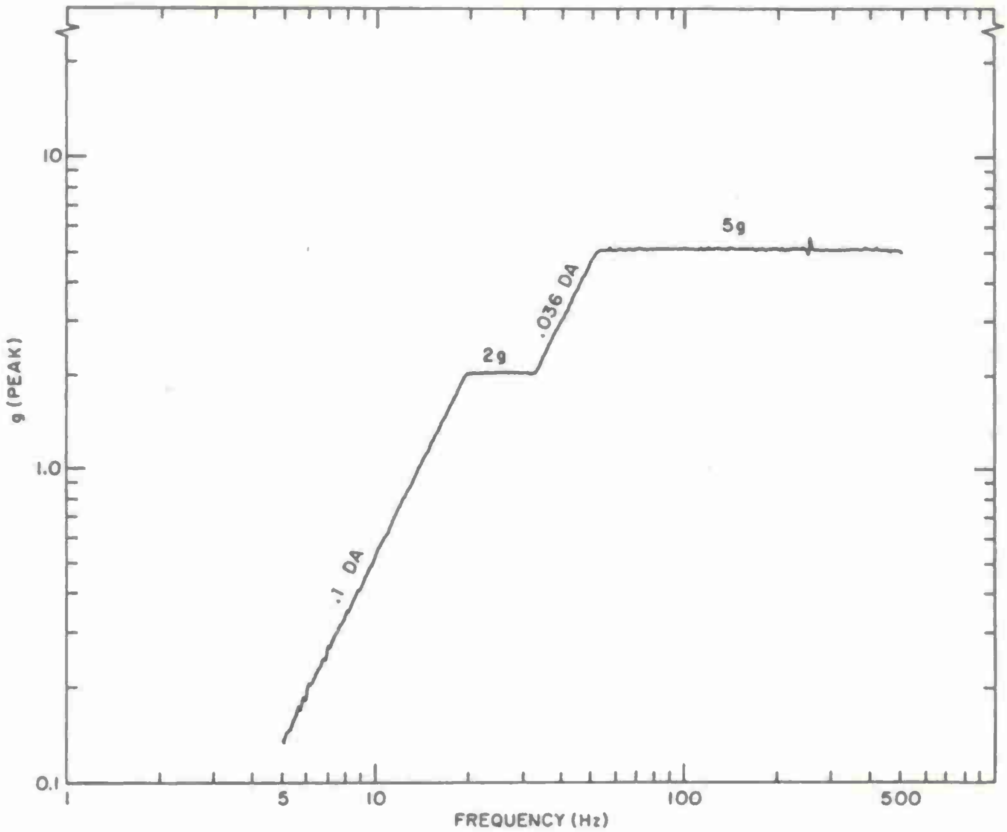


Figure 21. Amplitude voltage plot for test No. 6.
(all curves were "traced from original data.")

Test No: 7 Date: 10-5-73 Figure 22
Test ID: MIL-STD-810B

Figure: 514.1-4 Curve: C

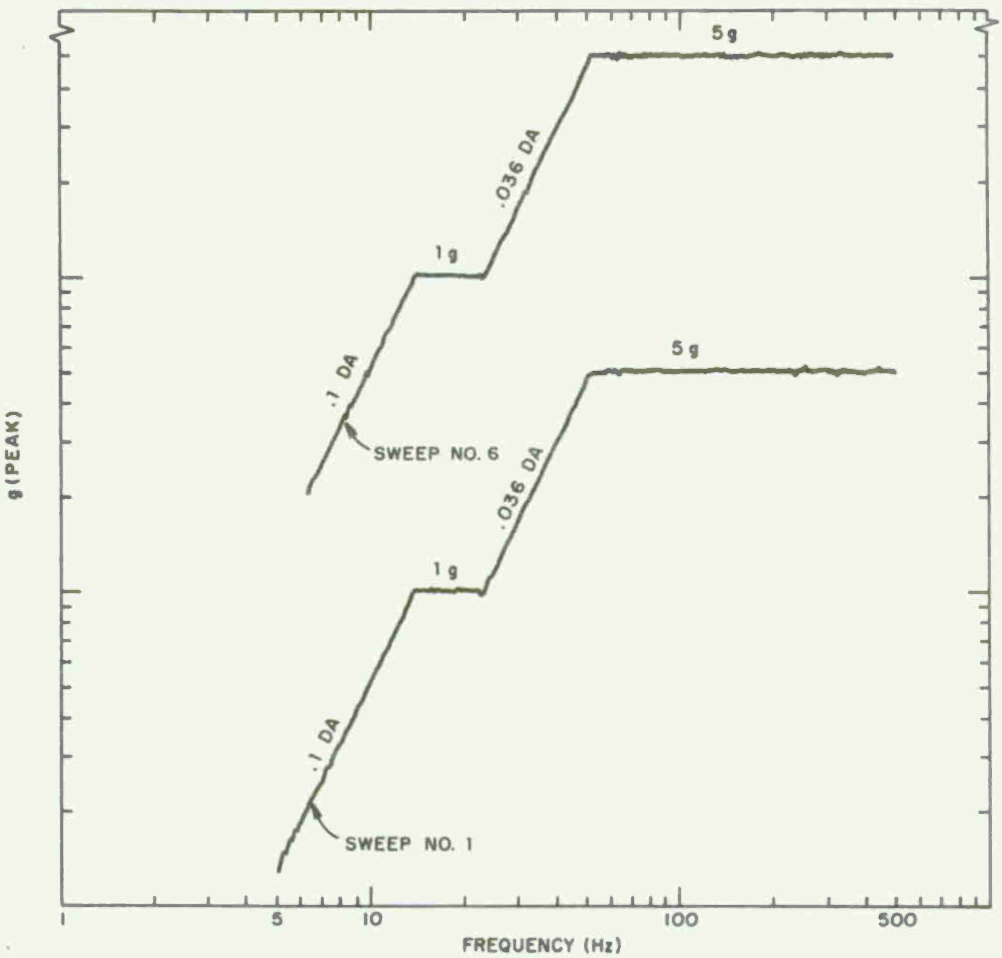


Figure 22. Amplitude voltage plot for test No. 7.

Test No: 8 Date: 10-9-73 Figure 23
Test ID: MIL-STD-810B

Figure: 514.1-4 Curve: H

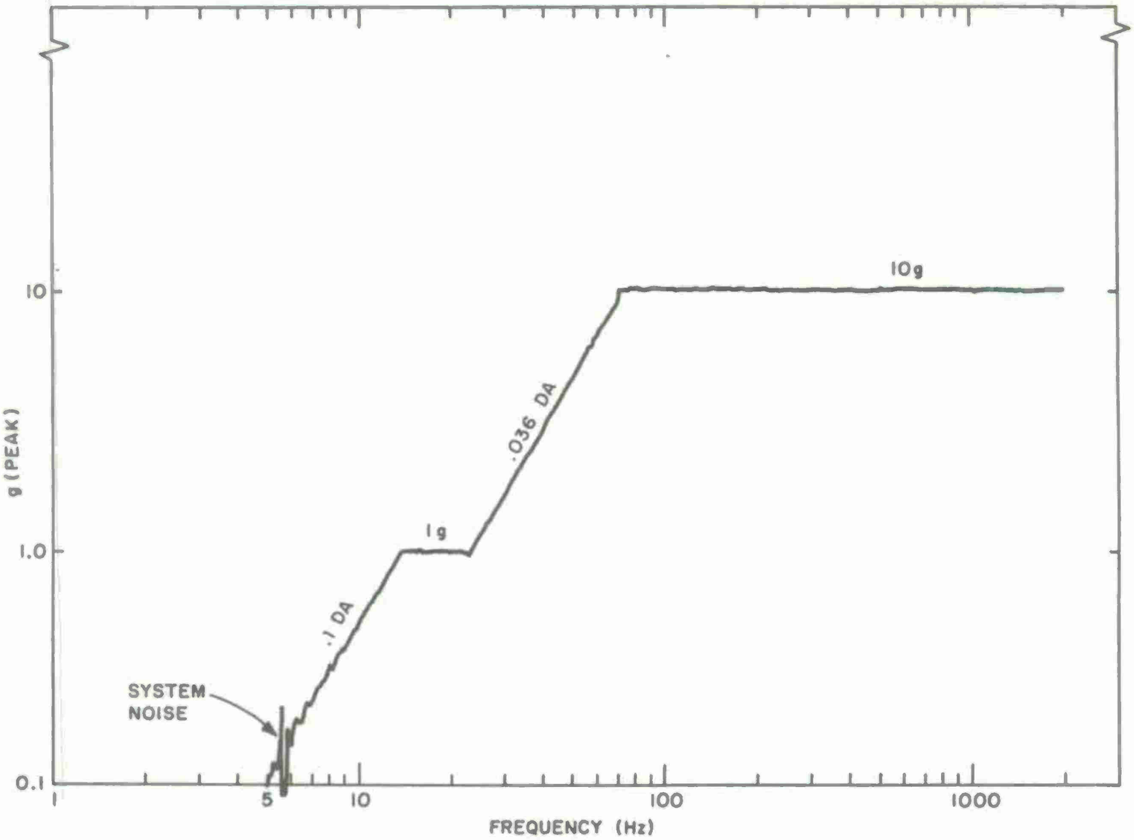


Figure 23. Amplitude voltage plot for test No. 8.
(all curves were "traced from original data.")

Test No: 9 Date: 10-10-73 Figure 24
Test ID: MIL-STD-810B

Figure: 514.1-4 Curve: AR

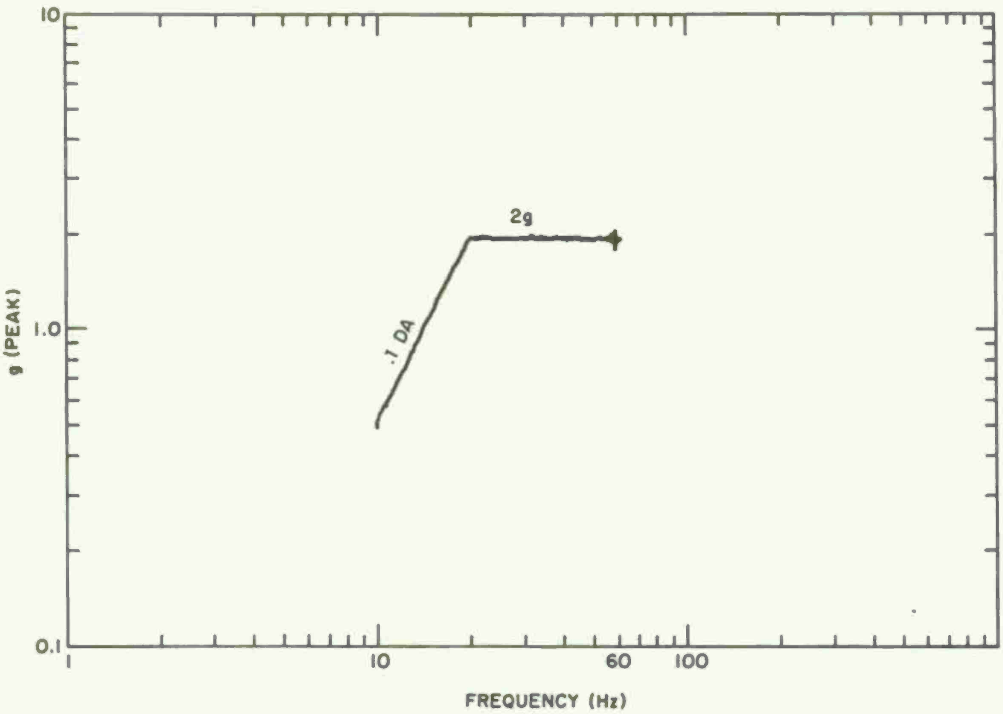


Figure 24. Amplitude voltage plot for test No. 9.
(all curves were "traced from original data.")

Test No: 10 Date: 10-11-73 Figure 25
Test ID: MIL-STD-810B

Figure: 514.1-4 Curve: N

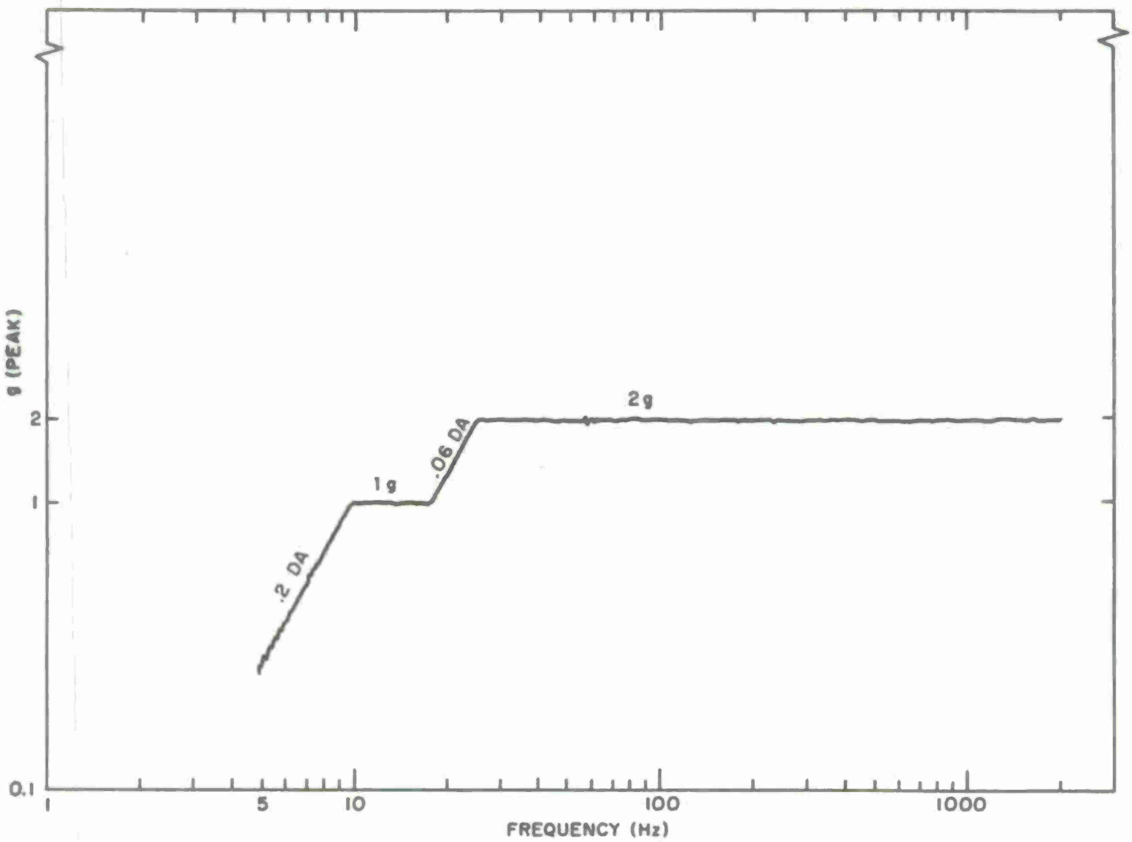


Figure 25. Amplitude voltage plot for test No. 10.
(all curves were "traced from original data.")

Test No: 11 Date: 10-11-73 Figure 26
Test ID: MIL-STD-810B

Figure: 514.1-5 Curve: P

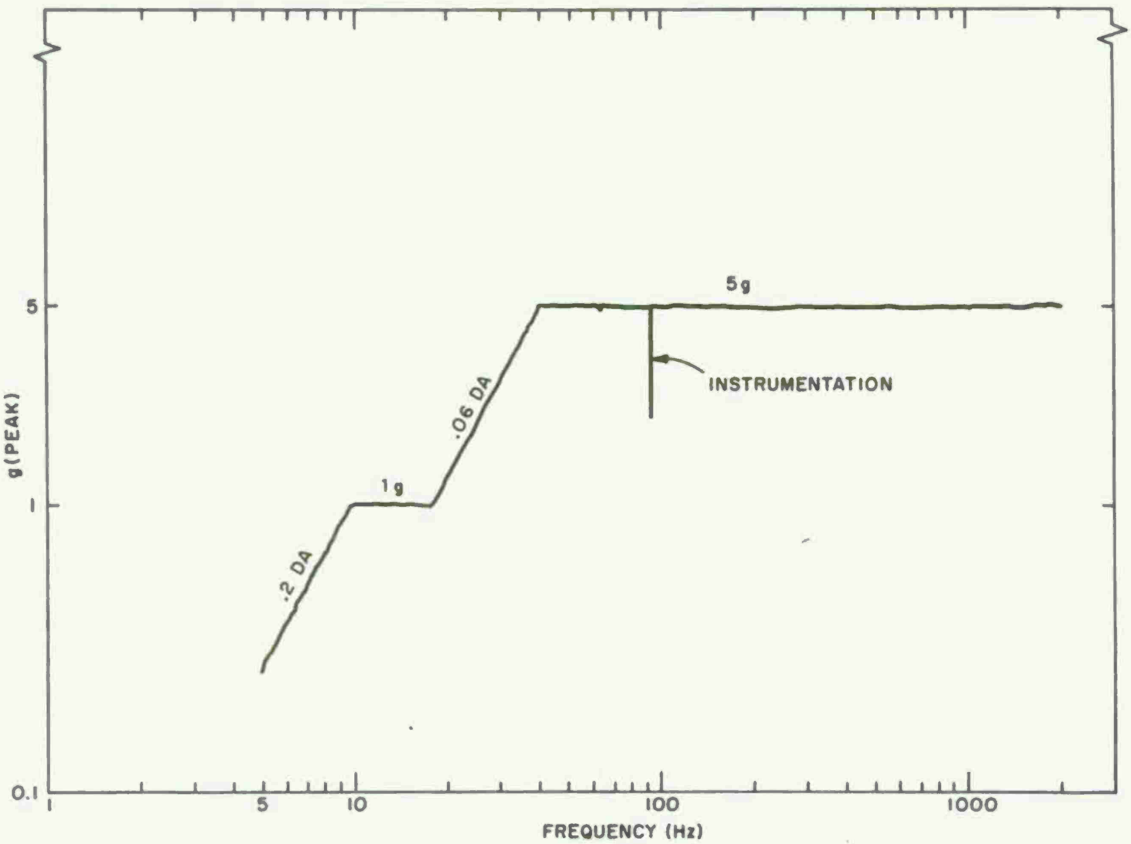


Figure 26. Amplitude voltage plot for test No. 11.
(all curves were "traced from original data.")

Test No: 12 Date: 10-12-73 Figure 27
Test ID: MIL-STD-810B

Figure 514.1-5 Curve: U

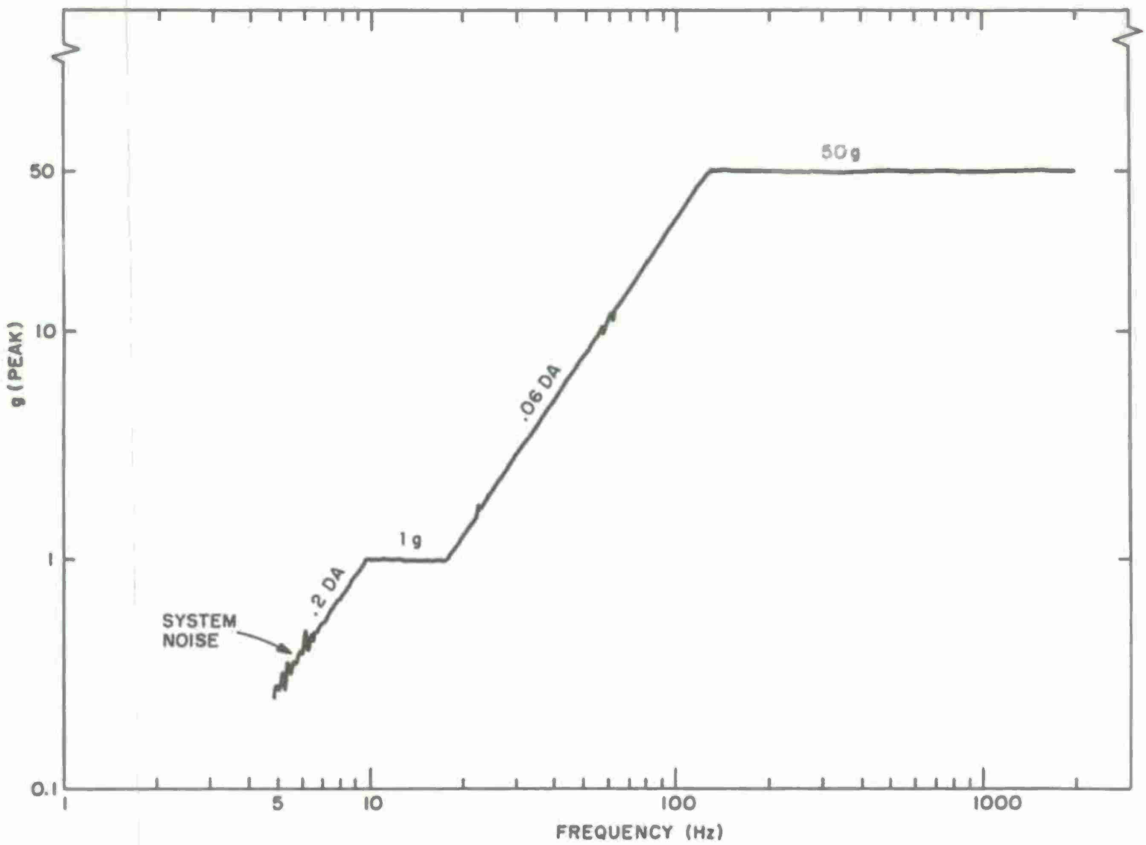


Figure 27. Amplitude voltage plot for test No. 12.
(all curves were "traced from original data.")

Test No: 13 Figure 28
Test ID: MIL-STD-810B

Figure: 514.1-6 Curve: V

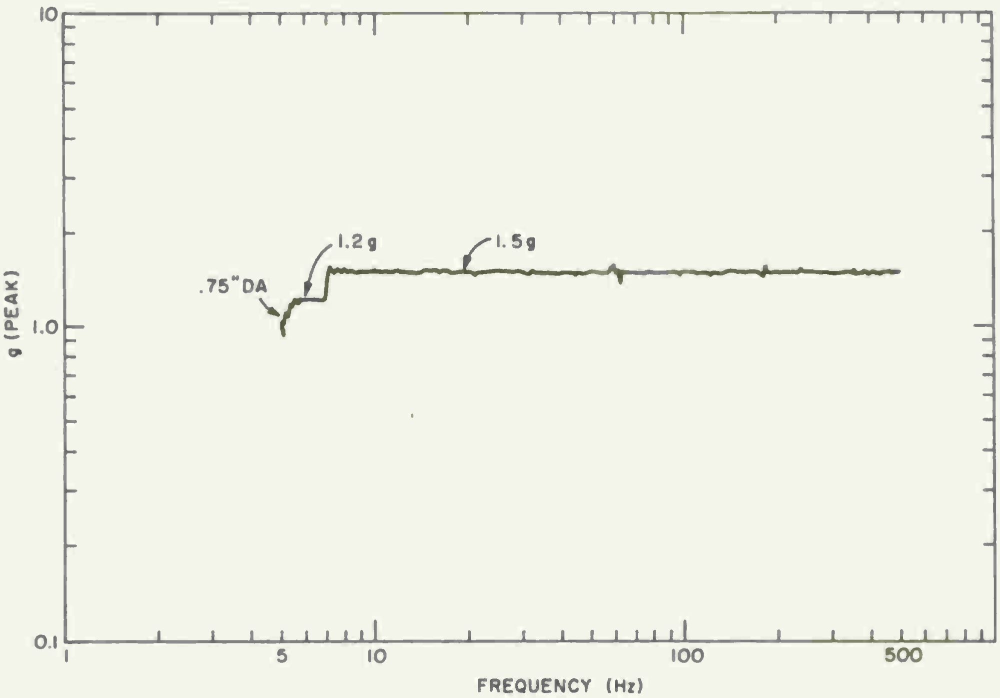


Figure 28. Amplitude voltage plot for test No. 13.
(all curves were "traced from original data.")

Test No: 14 Figure 29
Test ID: MIL-STD-810B

Figure 514.1-6 Curve: W

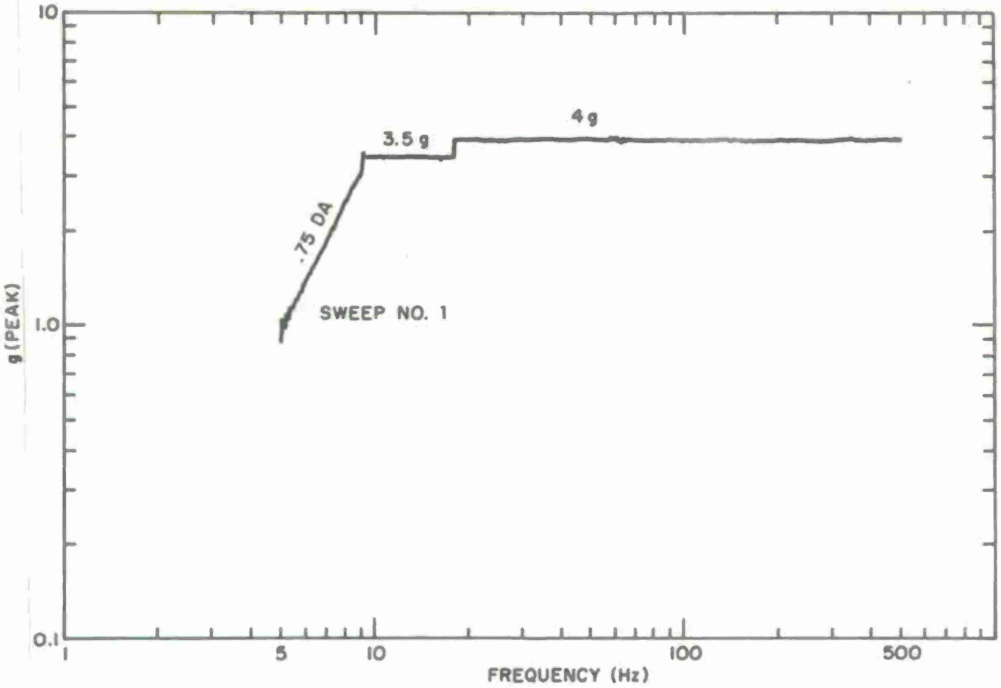


Figure 29. Amplitude voltage plot for test No. 14.
(all curves were "traced from original data.")

Test No: 15 Figure 30
Test ID: MIL-STD-810B

Figure: 514.1-7 Curve: AX

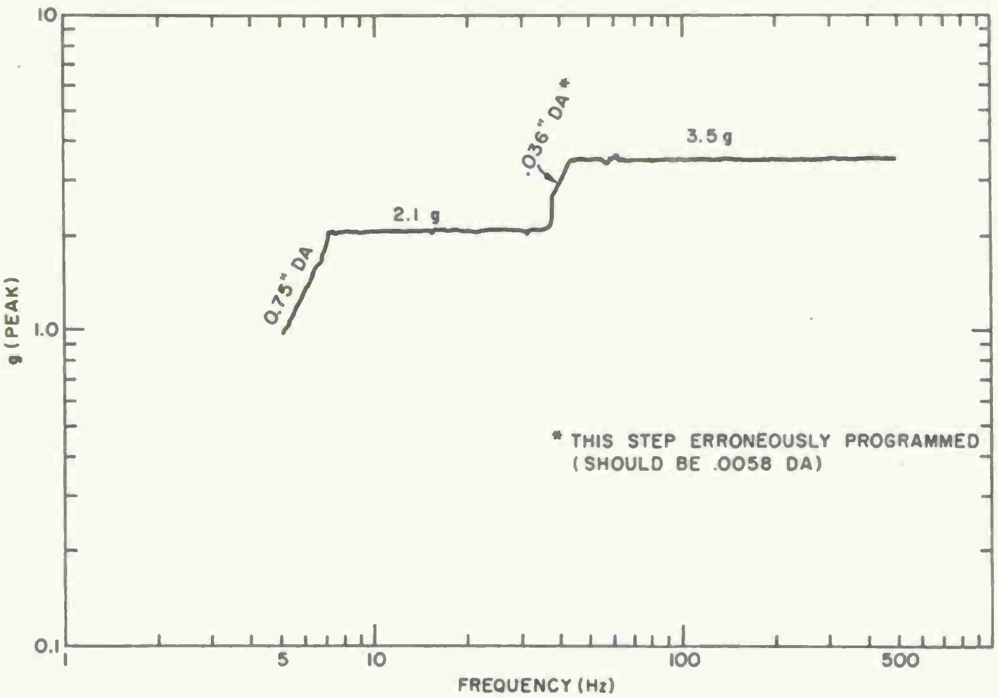


Figure 30. Amplitude voltage plot for test No. 15.
(all curves are "traced from original data.")

Test No: 16 Date: 10-17-73 Figure 31
Test ID: MIL-STD-810B

Figure: 514.1-7 Curve: AV

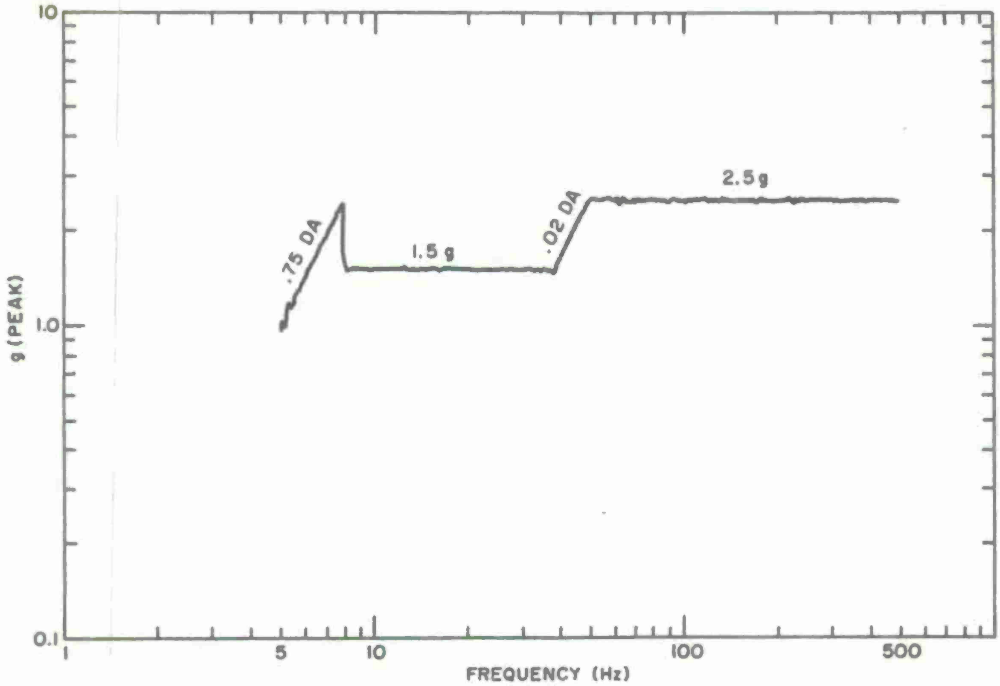


Figure 31. Amplitude voltage plot for test No. 16.

(all curves are "traced from original data.")

Test No: 17 Date: 10-24-73 Figure 32
Test ID: MIL-STD-331

Figure: Test 104
Para: 5.1.2.1

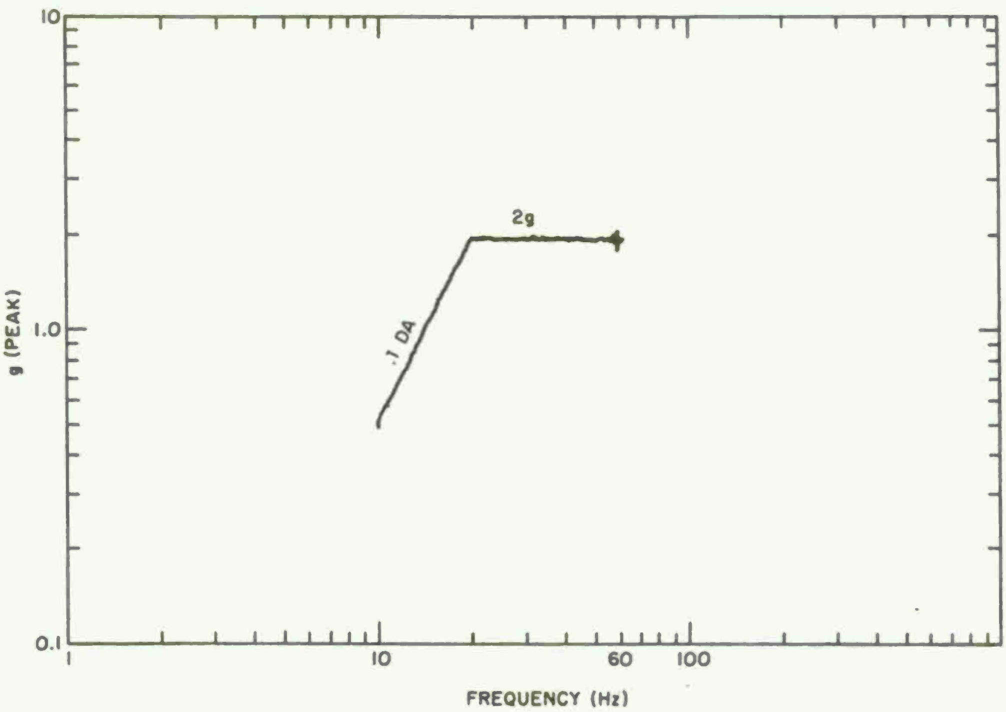


Figure 32. Amplitude voltage plot for test No. 17.
(all curves are "traced from original data.")

Test No: 18 Date: 10-24-73 Figure 33
Test ID: MIL-STD-331

Figure: Test 104
Para: 5.1.2.1

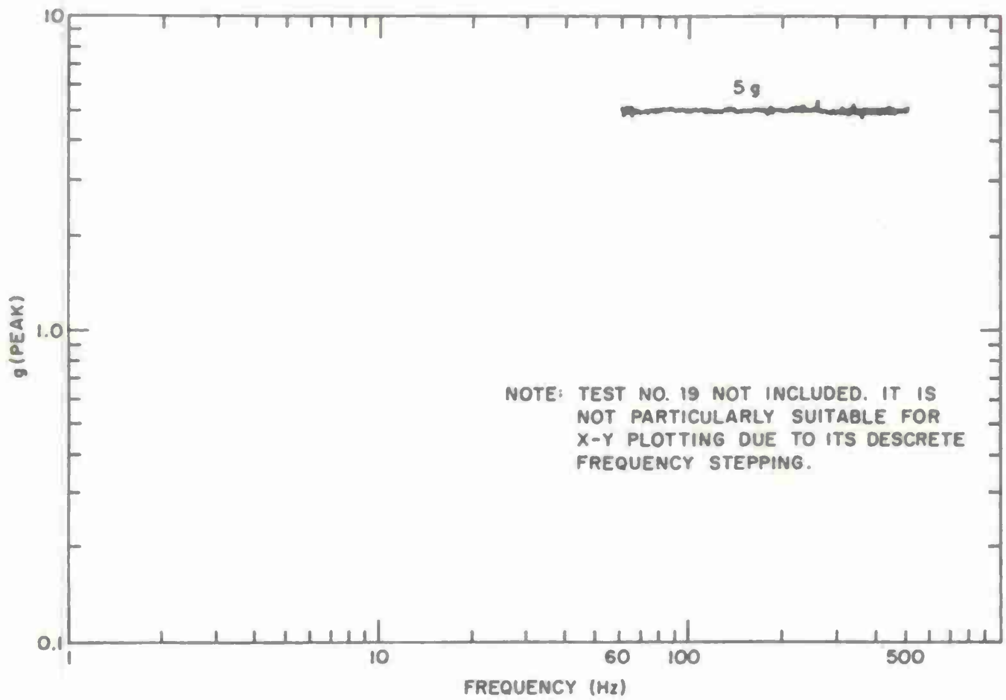


Figure 33. Amplitude voltage plot for test No. 18.

(all curves were "traced from original data.")

Test No: 20 Date: 11-7-73 Figure 34
Test ID: MIL-STD-331

Figure: Test 114
Para: 5.2.1

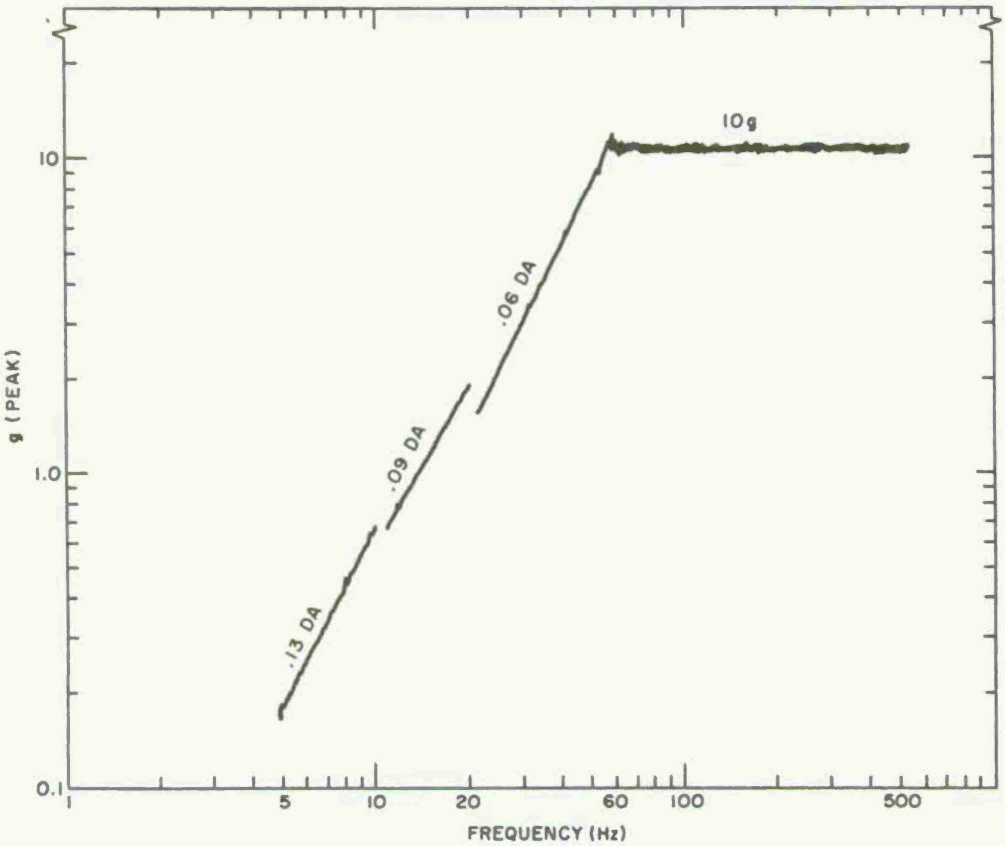


Figure 34. Amplitude voltage plot for test No. 20.

(all curves were "traced from original data.")

Test No: 21 Date: 11-7-73 Figure 35
Test ID: MIL-STD-810C (Proposed)

Figure: Attached Curve: A

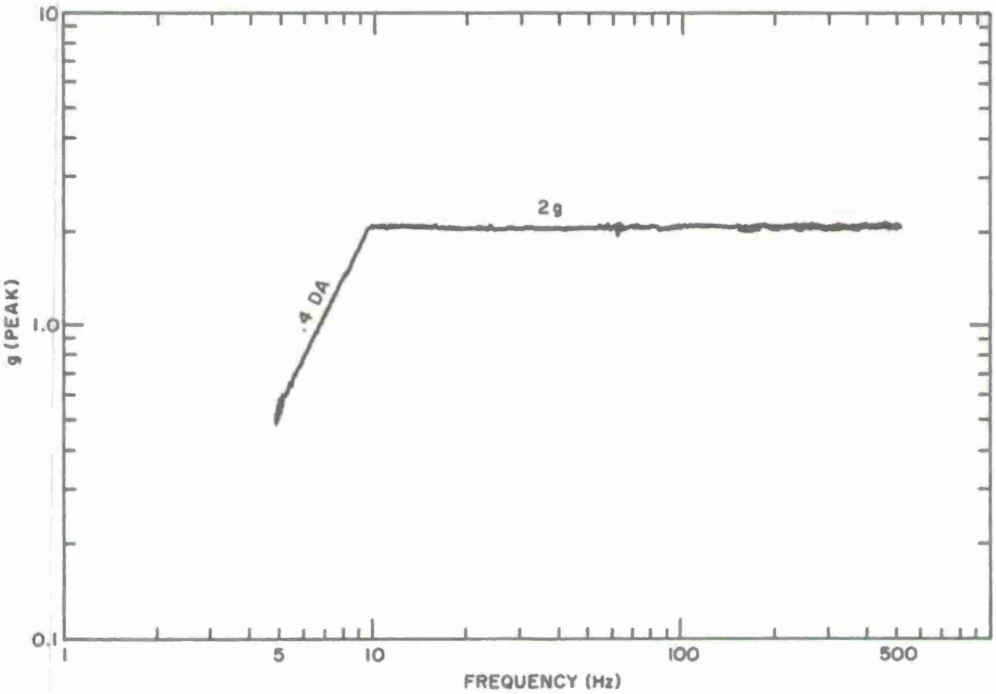


Figure 35. Amplitude voltage plot for test No. 21.
(all curves were "traced from original data.")

Test No: 22 Date: 11-7-73 Figure 36
Test ID: MIL-STD-810C (Proposed)

Figure: Attached Curve: B

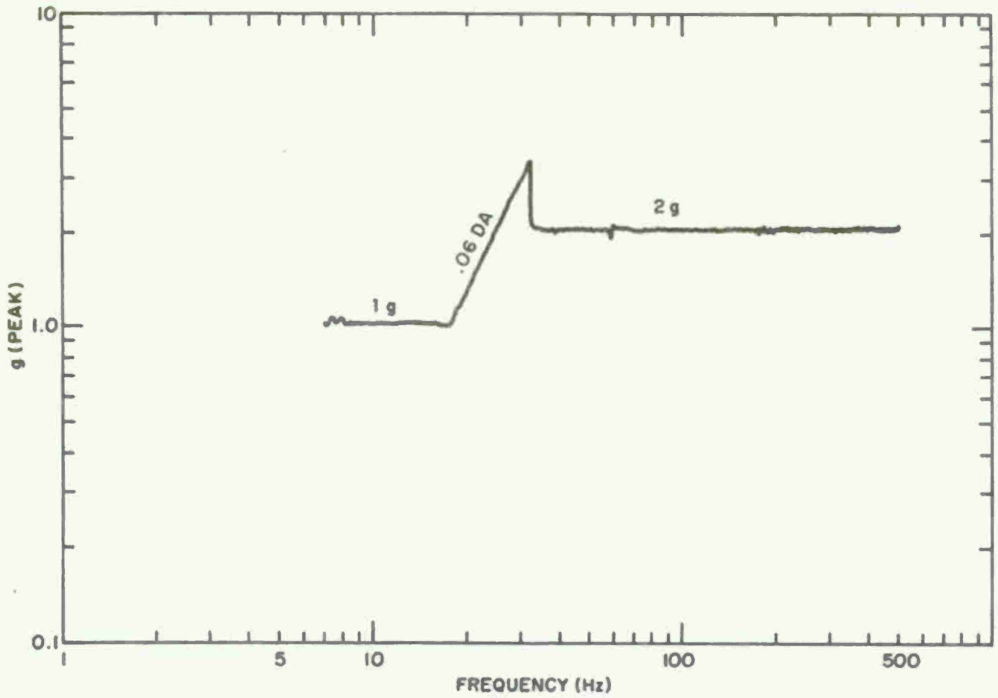


Figure 36. Amplitude voltage plot for test No. 22.

(all curves were "traced from original data.")

Test No: 23 Date: 11-7-73 Figure 37
Test ID: MIL-STD-810C (Proposed)

Figure: Attached Curve: C

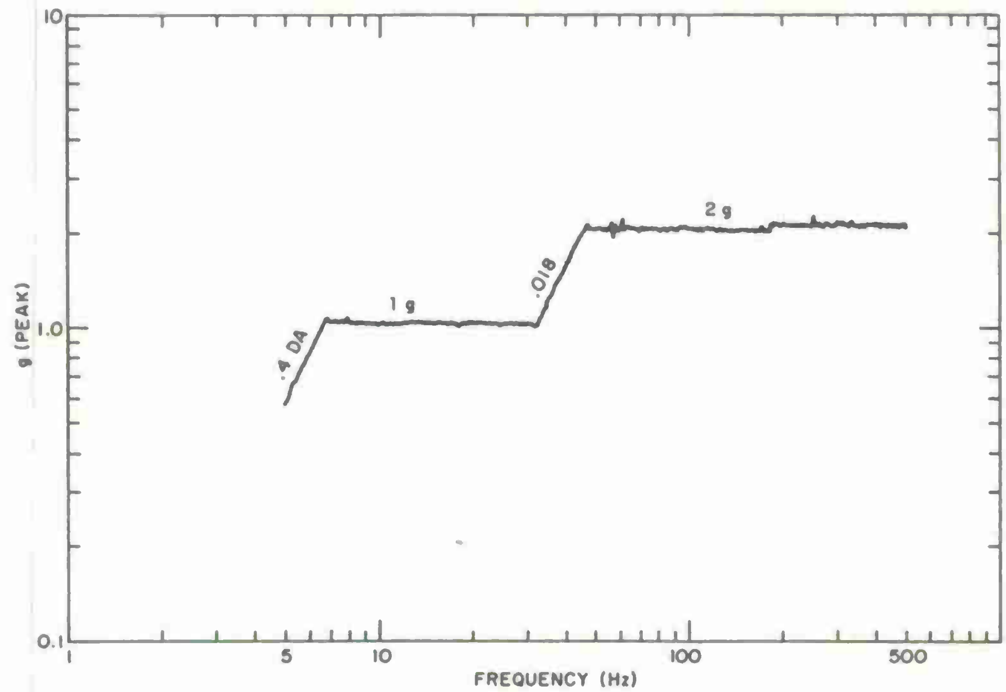


Figure 37. Amplitude voltage plot for test No. 23.
(all curves were "traced from original data.")

Attesting to the strength and responsiveness of the control loop was the DDC system's ability to control the test amplitude to the required ±10 percent during resonance condition.* Analog strip chart data (see sect 10.3) confirmed fixture/shaker resonance buildup between 1300 and 2000 Hz, a condition demanding a particularly fast response at 2000 Hz to comply with the accuracy requirements. A review of the data indicates that the test amplitude was controlled to +(7 ± 1) percent of the specified level at 2000 Hz. However, the ability of the DDC system to counteract resonance will depend, of course, on the specific test configuration. This example merely serves as an indication of the strength of the system's automatic compensation feature.

The amplitude stability of the DDC test system, particularly at low frequency (5 to 15 Hz), is further attested to by the plots of the digitized amplitude voltage versus frequency. These plots (figs. 16 through 37) display the (equivalent) peak acceleration voltage output of the transducer versus frequency for one-sweep cycle. Plotted on the y-axis is the digitized peak voltage from the control accelerometer (as processed by A/D converter and the computer) while frequency information shown on the x-axis is supplied by the excitation source, the D800 digital oscillator. The computer samples the data at the rate of 512 Hz and forwards the information to the plotter. The plotter maps the field (at a frequency optimized speed <<512 Hz) and linearly interpolates between adjacent points. Since the amplitude plot is logarithmic with frequency, displacement modes are represented by a constant positive voltage slope related to the quantity (XW^2) by the equation,

$$V_{out} = (XW^2) \sin wt$$

for which

$$(V_{out}) \max = [5.12 \times 10^{-2} (XW^2)] \times S.F. \frac{(mV\text{-}pk)}{g} \sim mV$$

where:

x ~ double amplitude displacement - in.

w ~ drive frequency - Hz

S. F. ~ voltage sensitivity factor - mV-pk/g

V ~ transducer output voltage - mV

**Manufacturer's data indicate a base table axial resonance of 4.3:1 at 2000 Hz. This was the maximum resonance in the 5 to 2000 band.*

Acceleration coordinates, on the other hand, are represented by zero slope lines whose magnitudes are proportional to the peak acceleration ($\ddot{X}$) expressed in G's

$$(V_{out})\ \max \;=\; \ddot{X}(g) \times \text{S. F.}\ \frac{(\text{mV-pk})}{g} \sim \text{mV}$$

Figures 16 through 37 portray stable control of the test amplitude for all tests performed. It can be quickly confirmed that control accuracy was maintained to well within ±10 percent over the entire frequency band (The only exceptions are random spikes brought about by extraneous noise, which cannot be eliminated completely, despite the increased transducer sensitivity; note also minor contributions from the ever present 60-Hz noise).

Amplitudes Error Computations.—— Amplitude-control accuracy was determined by comparing data from the control accelerometer against a reference (monitor) accelerometer. Data from the monitor accelerometer were obtained by using a highly accurate digital voltmeter, whereas the data for the control accelerometer were extracted from the teleprinter printout backed by the X-Y digitized amplitude voltage plots. (Computer printout data for the control accelerometer were available at every 1/3 octave point.) The availability of the computer printout data permitted a comparison between the average value of the test amplitude as executed and as requested. Furthermore, using extrapolation techniques backed by the digitized amplitude voltage plots, the instantaneous value of the test amplitudes recorded by both the monitor and control accelerometers at the same frequency can be extracted. Let curve A in figure 38 designate the required test reference, curves (B) and (C) designate the allowable ±10 percent envelope about curve (A). If the arbitrary point (X) designates the instantaneous amplitude as obtained from the control accelerometer, then the distance (X-Z) would represent the instantaneous error between the amplitude executed and value requested at a specific sweep frequency. However, to establish a basis for the accuracy of the control accelerometer in absolute terms, a highly accurate reference transducer was required. (Note that curve A is only a mathematical reference.) The monitor accelerometer providing data through the highly accurate digital voltmeter, was selected for that purpose. If

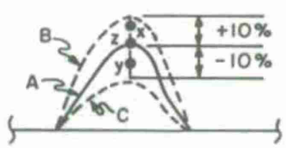


Figure 38. Total allowable error about test profile.

the arbitrary point (Y) depicts the instantaneous amplitude of this reference measurement, the absolute (control) error is given by the line connecting points (X, Z, Y), plus or minus the error associated with the reading tolerances of the DVM. This, then, is the total error that must be limited to less than or equal to ±10 percent per the test specifications. The expected value of the total error ($E_{T',e}$) can now be expressed as:

$$E_{T',e} = \left|(X, Z, Y)^2 + (\pm a)^2\right| 1/2$$

where:

(X, Z, Y) = Instantaneous differential reading between the monitor and control accelerometers,

a = Reading tolerances associated with the digital voltmeter.

The maximum total error, however, is obtained through linear combination of the preceding terms—that is,

$$E_{max} \leq \pm 10 \text{ percent} = (X, Z, Y) + (a)$$

The quantity (a) for the calibrated DVM was specified as follows for the 1.0-V full scale:

10 to 45 Hz: ±(.14 percent of reading + .02 percent of full scale)

The bulk of the tests were performed at acceleration levels below 15 g. Consequently, the total error due to reading tolerances was always below 0.5 percent as indicated below (monitor accelerometer sensitivity was 8.86 (mV-rms)/g:

$$a = \pm \frac{.14}{100} \times 8.86 \frac{\text{mV-rms}}{\text{G}} \times 15 \text{ g} + \frac{.02}{100} \times 1000 \text{ mV}$$

$$(a)_{max} \cong + .4 \text{ mV (rms)}$$

resulting in percent error equal to

$$\%(a)_{max} = \frac{.4 \text{ mV rms} \times 100\%}{8.86 \frac{\text{mV rms}}{\text{G}} \times 15 \text{ g}} \cong 0.3\%$$

For the case of maximum acceleration (50 g), the error is even smaller:

$$(a)_{max} = + \frac{.04 \times 8.86 \frac{\text{mV-rms}}{\text{G}} \times 50\ \text{G}}{100} + .2\ \text{mV} \cong + .4\ \text{mV-rms}$$

$$\%(a) = \frac{.4\ \text{mV}}{8.86 \times 50} \times 100 \cong .10\%$$

Since 10 percent >> 0.3 percent, errors due to DVM reading tolerances can be neglected. Accordingly, the errors being computed can now be expressed as follows:

$$E_{cm} = 100 \frac{[\text{Test Amplitude (Control) - Test Amplitude (Monitor)}]}{\text{Test Amplitude (Monitor)}} \sim \% \quad (19)$$

$$E_{CR} = 100 \frac{[\text{Test Amplitude (Control) - Test Amplitude (Reference)}]}{\text{Test Amplitude (Reference)}} \sim \% \quad (20)$$

where E_{cm} = percent error in test amplitude based on the instantaneous difference data between the control and monitor measurements. It is this quantity that expresses the amplitude control accuracy and must be less than or equal to ±10 percent.

E_{CR} = percent error in test amplitude based on the instantaneous difference data between the control accelerometer and the specified test reference. This quantity will typically be less than or equal to ±1.0 percent. Note that the errors as defined above refer to either displacement or acceleration modes, as all amplitudes are converted to voltage values. Data from all tests were analyzed in accordance with equations (19) and (20) and summarized in tables VII through XXVII. In most cases, at least three frequencies were selected for each test mode. Since the DVM is limited to 10 Hz, data obtained for the monitor accelerometer at 10 and 11 Hz are questionable.

If Em-r is defined as the instantaneous error between monitor accelerometer and the specified test reference, then this quantity can be easily determined from the following relationships:

$$\pm \text{Ec-r} \pm \text{Ec-m} = \text{Em-r};$$

but since Ec-r << Ec-m,

$$\text{Emr} \cong |\text{Ec-m}| \ .$$

10.2 Frequency-Control Accuracy

The frequency-control requirements invoked by the individual specifications are given as follows:

MIL-STD-810B	±2 percent of specified value or ±1/2 Hz below 20 Hz
MIL-STD-331	±3 percent of specified value

To demonstrate compliance with these requirements,* the DDC test system was programmed for a 60 sec, 15-g** acceleration dwell at each octave band within the 5- to 2000-Hz band. Two frequency counters were connected to the control accelerometer (mounted per description in 9.2) to record the excitation frequency. Data from these counters are presented in table XXVIII at selectable programmed frequencies. Frequency-control error analysis, based on these test data, affirms the capability of the digital oscillator to synthesize and control the test frequencies well within the specified values. The data indicate that the DDC test system was able to control the test frequency to within ±.1 percent at 5 Hz, and to within less than ±.2 percent in the frequency band of 20 to 2000 Hz. On a per cycle basis, the test frequency was controlled to within ±.05 Hz below 20.0 Hz, an order of magnitude improvement over the specification requirements.

The highly accurate (±1 count error) frequency counters were used as standard references for comparison against the programmed frequencies. Frequency-control accuracy (that is, frequency error) was determined from the following relationships:

$$E_f = 100 \times \frac{[Fc-Fp]}{Fc} \sim \%$$

where:

E_f = Frequency-error percent

F_c = Control accelerometer test frequency measured by the frequency counters (Hz)

F_p = DDC test system programmed frequency (Hz).

**These frequency control requirements are typical to most military vibration tests standards.*

***The g-acceleration dwell was modified as required to comply with systems limitations.*

TABLE XXIX. FREQUENCY ACCURACY DATA* (DATA TAKEN 2 NOV 1973)

Programmed dwell		Measured frequency				
Frequency (Hz)	Acceleration (g)	Direct frequency counter 1 (Hz)	Inverse frequency counter No. 2 (Hz^{-1})	Frequency counter 2 (Hz)	Frequency ±1 counter error - counter No. 2 (Hz)	Maximum percent error programmed frequency versus measured frequency from No. 2 counter
5.0	.90	5.0	199.81×10^{-3}	5.005	~0	~.10
10.0	.90	10.0	100.50×10^{-3}	9.95	~0	0.50
21.0	15.0	21.0	47.615×10^{-3}	21.00	~0	0
40.0	15.0	40.0	25.000×10^{-3}	40.00	~0	0
80.0	15.0	80.0	12.500×10^{-3}	80.00	.0065	~0
160.00	15.0	160.0	6.250×10^{-3}	160.00	.025	.016
320.0	15.0	320.0	3.125×10^{-3}	320.00	.110	.034
640.0	15.0	640.0	1.563×10^{-3}	639.79	.41	.09
1280.0	15.0	-	0.781×10^{-3}	1280.41	2.40	.22
2000.0	15.0	-	0.500×10^{-3}	2000.00	4.0	0.20

*No. 1 Counter: General Radio model 1191B (HDL 34068); 1.0-sec data gate, 1.0-sec display time. Accuracy ±1 count.

No. 2 Counter: Hewlett Packard 5212A electronic counter (HDL 25307); valid calibration Aug 1973 to Feb 1974; Accuracy ±1 count.

10.3 Strip-Chart Data, Computer Printouts, and Digital Synthesizer Waveform Data

This section contains raw test data for selective tests as obtained from real-time computer printouts (tables XXIX through XXXIII), analog records of accelerometer voltage versus frequency (figs. 39-43), and photographic records of the digitally synthesized sinusoidal driving waveform (figs. 44-47). Selective data are presented for tests 3, 4, 9, 17 and 18.*

10.3.1 Computer Printout

This computer record consists of three parts. The first one contains a summary of test identification, test-profile information, and ALARM/ABORT limits. Test levels are expressed as double-amplitude displacement D (in in.) or acceleration A (in g's); frequencies are given in Hz, and ALARM/ABORT limits permanently set at ±.929/3.0 dB, where ±.92 dB corresponds to ±10 percent. Test time, number of sweep cycles, and sweep speed are expressed in minutes, Hz, and octaves/min, respectively.

The second part of this record consists of a real-time computer printout of the test mode as it is being executed versus the requested profile. Columns marked 1 through 6 in this printout (see table XXIX) are identified as follows:

Column 1 - Identifies the 1/3 octave point at which printout is provided. CR stands for crossover point, AL for alarm message (which is printed whenever amplitude control exceeds ±10 percent). The computed value of the test amplitude is averaged over 1/2-2.0 sec of data time prior to and including the indicated test time.

2 - Designates channel No. 8.

3 - Identifies the (average) magnitude of the test amplitude as it is being executed.

4 - Identifies test mode. A ≡ acceleration in g's. D ≡ displacement in inches (double amplitude). V ≡ velocity in in./sec.

5 - Lists the magnitude of the requested test profile.

6 - Lists the test frequency corresponding to the 1/3 frequency point.

7 - Lists cumulative test time from start (in min).

**Computer printout data and analog data are presented for tests 3, 4, 9, 17, and 18. More comprehensive photographic records are presented in section 10.3.3.*

The third part of this record consists of computer printout during the simulated resonance/dwell routine for the indicated test.

10.3.2 Analog Strip-Chart Data

Analog (voltage) strip-chart data for the indicated tests are presented in figures 39 through 43 for the control accelerometer, monitor accelerometer, and the two inplane (cross-talk) accelerometers. Also plotted is a d-c signal proportional to frequency to synchronize all measurements. The indicated voltages correspond to the rms value of the sinusoidal waveform. When set on linear mode (ac-dc selectable scale), the recorder has a flat response within ±1.0 dB (approx ±10 percent) over the frequency range of 10 to 100 kHz. Since this error is on the order of accuracy sought for the control accelerometer, such data can serve only as a backup record, quickly informing the operator of inconsistencies in amplitude repeatability, or of the existence of noise or resonance in the exciter/specimen combination. It can also be used to determine the slope of the displacement or acceleration profile to demonstrate that no dropoff (or drift) exists in the test amplitude. Since the rms voltage output of the accelerometer is proportional to its excitation, constant acceleration levels would appear as straight lines (that is, constant voltage ±10 percent). This is based on the fact that the output voltage is proportional to the product of the sensitivity factor and the acceleration

$$V_{out} = \text{S. F. } (V/g)\ \ddot{X}(g)$$

where:

V_{out} = Voltage output

S. F. = Accelerometer sensitivity factor in Vrms/g

$\ddot{X}$ = Acceleration level in g's

The output voltage corresponding to a displacement mode would appear as a second-order curve based on the relationships:

$$V_{out} = \text{S. F. } \left(\frac{\text{V-rms}}{g}\right)(C \cdot X \cdot W^2) \sim \text{volts}$$

where:

C = Conversion factor - 5.12×10^{-2}

X = Double-amplitude displacement (in.)

W = Input frequency - Hz

TABLE XXX. COMPUTER PRINTOUT OF TEST NO. 3

```
ID0       IDENTIFICATION
          #LINES          5

ID1       SINE TEST
          MIL-STD-810B, 20, OCT. 1973, FIG.514.1-2, CURVE (C)

ID2       TEST DESCRIPTION LINE 1
          5HZ-14HZ .1DA, 14HZ-23HZ 1G 23HZ-52HZ .036D ,52HZ-500HZ

ID3       TEST DESCRIPTION LINE 2
          5G'S TOTAL TEST TIME 3HRS. LESS DWELL TIMTE

ID4       DATE
          SEPT 24, 1973 DWELL AT 5HZ FOR 30MINS

ID5       PREPARED BY
          D.R.BRYANT

IS0       INPUT SIGNALS
          #LINES          1

          XDUCER TYPE  A,V,D  A

IS1       ACCEL. SENS.                 30.02  <-- Adjusted to 100 mV-pg/g to
          MUX PORT                      0         increase signal/noise ratio
          AVERAGE                N
          LEVEL RATIO                   1
          SELECT-LO              N
          SELECT-HI              Y
          DISPLAY                Y
          TRACK                  Y

FR0       FREQUENCIES
          #LINES          4

FR1       F LOW           5

FR2       F HIGH        500

FR3       F START         5

FR4       F START INCREASING Y

AP0       AMPLITUDE PROFILE
          #LINES          4

AP1       AMPL        9.99 E-02
          A,V,D       D
          INPUT F     N
          F               5
          ALARM            .919
          ABORT           3

AP2       AMPL            1
          A,V,D       A
          INPUT F     Y
          F              14
          ALARM            .919
          ABORT           3
```

TABLE XXX. COMPUTER PRINTOUT OF TEST NO. 3 (CONT'D)

```
AP3     AMPL        3.59  E-02
        A,V,D       D
        INPUT F     Y
        F              23
        ALARM            .919
        ABORT            3

AP4     AMPL             5
        A,V,D       A
        INPUT F     Y
        F              52
.       ALARM            .919
        ABORT            3

TD0     TEST DURATION
        #LINES           1

TD1     TIME        Y
        TIME         150
        SWP CYCLES            Y
        N              10
        SWP SPD     N
        SPEED            .835
        SPECIMEN Q
        L,M,H       L

1    2        3     4        5        6        7
>
UP   8      .103    D      .100      5         0
>SU
>
UP   8      .101    D      .100      5         .117
>
1/3  8      .102    D      .100      5.33      .217
>
1/3  8      .101    D      .100      6.32      .5
>
1/3  8      .101    D      .100      8.02      .833
>
1/3  8      .100    D      .100      10.0      1.25
>
1/3  8      .101    D      .100      12.7      1.63
>
CR   8      .100    D      .100      13.9      1.77
>
1/3  8      1.01    A      1         16.0      2
>
1/3  8      1.00    A      1         20.2      2.38
>
CR   8      1       A      1         22.9      2.59
>
1/3  8  3.61 E-02   D 3.59 E-02      25.4      2.75
>
1/3  8  3.61 E-02   D 3.59 E-02      32.1      3.13
>
1/3  8  3.60 E-02   D 3.59 E-02      40.4      3.5
>
1/3  8  3.60 E-02   D 3.59 E-02      50.9      3.88
>
CR   8  3.60 E-02   D 3.59 E-02      52        3.91
```

Column Definition

1 - PR≡Print
2 - Channel No. 8
3 - Test Amplitude
4 - D≡Displacement ("DA)
    A≡Acceleration (g)
5 - Test Amplitude
    Requested
6 - Frequency (Hz)
7 - Time (Min)

TABLE XXX. COMPUTER PRINTOUT OF TEST NO. 3 (CONT'D)

>							
1/3	8	5.06	A	5	64.1	4.25	
>							
1/3	8	5	A	5	80.9	4.63	
>							
1/3	8	5	A	5	101	5.02	
>							
1/3	8	4.97	A	5	128	5.38	
>							
1/3	8	4.98	A	5	162	5.75	
>							
1/3	8	4.98	A	5	204	6.13	
>							
1/3	8	4.98	A	5	257	6.5	
>							
1/3	8	5	A	5	323	6.88	
>							
1/3	8	4.98	A	5	408	7.25	
>							
CR	8	4.98	A	5	500	7.58	Upsweep to 500 Hz
>							
1/3	8	5	A	5	405	7.91	Downsweep to 5 Hz
>							
1/3	8	4.98	A	5	321	8.28	
>							
1/3	8	4.86	A	5	255	8.69	~ T+7.5 Min
>							
1/3	8	4.98	A	5	202	9.03	
>							
1/3	8	4.98	A	5	161	9.41	
>							
1/3	8	5	A	5	128	9.78	
>							
1/3	8	4.97	A	5	101	10.1	
>							
1/3	8	4.98	A	5	80.4	10.5	
>							
1/3	8	4.91	A	5	63.8	10.9	
>							
CR	8	5	A	5	52.0	11.3	
>							
1/3	8	3.59 E-02	D	3.59 E-02	48.9	11.3	
>							
1/3	8	3.58 E-02	D	3.59 E-02	40.2	11.6	
>							
1/3	8	3.58 E-02	D	3.59 E-02	32	12	
>							
1/3	8	3.59 E-02	D	3.59 E-02	25.4	12.4	
>							
CR	8	3.56 E-02	D	3.59 E-02	23.0	12.5	
>							
1/3	8	.994	A	1	20.1	12.8	
>							
1/3	8	.998	A	1	16.0	13.1	
>							
CR	8	.994	A	1	14.0	13.3	
>							
1/3	8	9.96 E-02	D	.100	12.7	13.5	

TABLE XXX. COMPUTER PRINTOUT OF TEST NO. 3 (CONT'D)

```
>
1/3 8 9.96 E-02  D    .100   10.0    13.9
>
1/3 8 9.96 E-02  D    .100    8.02   14.2
>
1/3 8 9.99 E-02  D    .100    6.33   14.6
>
AL  8 9.11 E-02  D    .100    5.61   14.8
>                                            End 1st cycle
1/3 8 9.81 E-02  D    .100    5.05   15      ~T+15.0 min
>
CR  8 9.81 E-02  D    .100    5      15
>
```

TABLE XXXI. COMPUTER PRINTOUT OF TEST NO. 4

```
ID0       IDENTIFICATION
          #LINES        5

ID1       SINE TEST
          MIL STD810B  20,OCT 1969 FIG514.1-2, CURVE (H)

ID2       TEST DESCRIPTION LINE 1
          5HZ-14HZ .1DA 14HZ-23HZ 1G 23HZ-74HZ .036DA 74HZ-2000HZ 10G'

ID3       TEST DESCRIPTION LINE 2
          TOTAL TEST TIME 3HRS LESS 30 MIN DWELL AT 2000HZ

ID4       DATE
          SEPT 24, 1973

ID5       PREPARED BY
          D.RBRYANT

IS0       INPUT SIGNALS
          #LINES        1

          XDUCER TYPE  A,V,D  A

IS1       ACCEL. SENS.          30.92 <-- Adjusted to 100 mV-pk/g
          MUX PORT              0         to increase signal/noise ratio
          AVERAGE            N
          LEVEL RATIO           1
          SELECT-LO          N
          SELECT-HI          Y
          DISPLAY            Y
          TRACK              Y

FR0       FREQUENCIES
          #LINES        4

FR1       F LOW         5

FR2       F HIGH     2000
```

TABLE XXXI. COMPUTER PRINTOUT OF TEST NO. 4 (CONT'D)

```
FR3       F START        5

FR4       F START INCREASING Y

AP0       AMPLITUDE PROFILE
          #LINES         4

AP1       AMPL       9.99 E-02
          A,V,D      D
          INPUT F    N
          F              5
          ALARM           .919
          ABORT          3

AP2       AMPL           1
          A,V,D      A
          INPUT F    Y
          F             14
          ALARM           .919
          ABORT          3

AP3       AMPL       3.59 E-02
          A,V,D      D
          INPUT F    Y
          F             23
          ALARM           .919
          ABORT          3

AP4       AMPL          10
          A,V,D      A
          INPUT F    Y
          F             74
          ALARM           .919
          ABORT          3

TD0       TEST DURATION
          #LINES         1

TD1       TIME       Y
          TIME         150
          SWP CYCLES          Y
          N              7.5
          SWP SPD    N
          SPEED           .863
          SPECIMEN   Q
          L,M,H      L
OK
>
TY  CH   LEVEL  AVD REFERENCE  FREQ-HZ  MIN
>
UP   8     .100  D      .100     5         0
>
1/3  8     .101  D      .100     5.26      0
>
AL   8     .105  D      .100     5.73       .233
>
1/3  8     .104  D      .100     6.3
```

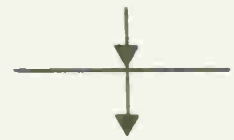
TABLE XXXI. COMPUTER PRINTOUT OF TEST NO. 4 (CONT'D)

AL	8	.104		D	.100		6.59	.467
>								
1/3	8	.103		D	.100		7.96	.783
>								
AL	8	.105		D	.100		8.55	.900
>								
1/3	8	.104		D	.100		10	1.17
>								
1/3	8	.104		D	.100		12.6	1.57
>								
CR	8	.104		D	.100		14	1.73
>								
1/3	8	1.00		A	1		16.0	1.97
>								
1/3	8	1.00		A	1		20.2	2.37
>								
CR	8	1.00		A	1		22.9	2.59
>								
1/3	8	3.60	E-02	D	3.59	E-02	25.4	2.75
>								
1/3	8	3.61	E-02	D	3.59	E-02	32.1	3.15
>								
1/3	8	3.59	E-02	D	3.59	E-02	40.4	3.53
>								
1/3	8	3.59	E-02	D	3.59	E-02	51	3.94
>								
1/3	8	3.64	E-02	D	3.59	E-02	64.1	4.31
>								
CR	8	3.59	E-02	D	3.59	E-02	73.9	4.56
>								
1/3	8	10		A	10		80.9	4.70
>								
1/3	8	10		A	10		101	5.09
>								
1/3	8	9.97		A	10		128	5.48
>								
1/3	8	10		A	10		161	5.88
>								
1/3	8	10		A	10		203	6.27
>								
1/3	8	10		A	10		257	6.66
>								
1/3	8	10		A	10		323	7.05
>								
1/3	8	10		A	10		408	7.44
>								
1/3	8	9.94		A	10		513	7.83
>								
1/3	8	9.97		A	10		647	8.22
>								
1/3	8	10		A	10		816	8.59
>								
1/3	8	9.97		A	10		1020	8.97
>								
1/3	8	9.97		A	10		1290	9.38
>								
1/3	8	9.97		A	10		1630	9.78

Upsweep to 2000 Hz

T+10.0

CR	8	10	A	10	2000	10.0
1/3	8	9.97	A	10	1620	10.4
1/3	8	10	A	10	1280	10.8
1/3	8	10	A	10	1020	11.3
1/3	8	10	A	10	810	11.6
1/3	8	10	A	10	641	12.0
1/3	8	10	A	10	510	12.4
1/3	8	10	A	10	405	12.8
1/3	8	10	A	10	321	13.2
1/3	8	9.81	A	10	255	13.6
1/3	8	9.94	A	10	202	14
1/3	8	10	A	10	161	14.3
1/3	8	10	A	10	128	14.8
1/3	8	9.97	A	10	101	15.2
1/3	8	9.97	A	10	80.4	15.5
CR	8	9.97	A	10	74	15.7
1/3	8	3.55 E-02	D	3.59 E-02	63.8	16
1/3	8	3.58 E-02	D	3.59 E-02	50.7	16.3
1/3	8	3.56 E-02	D	3.59 E-02	40.1	16.7
1/3	8	3.56 E-02	D	3.59 E-02	31.9	17.1
1/3	8	3.58 E-02	D	3.59 E-02	25.3	17.5
CR	8	3.56 E-02	D	3.59 E-02	23.0	17.6
1/3	8	.994	A	1	20.1	17.9
1/3	8	.998	A	1	16.0	18.3
CR	8	.992	A	1	14.1	18.5
1/3						
AL	8	9.50 E-02	D	.100	12.6	18.7
1/3	8	9.64 E-02	D	.100	10.1	19



Downsweep to 5 Hz

TABLE XXXI. COMPUTER PRINTOUT OF TEST No. 4 (CONT'D)

> 1/3	8	9.64	E-02	D	.100	7.98	19.4	
> AL	8	9.45	E-02	D	.100	7.51	19.6	
> 1/3	8	9.33	E-02	D	.100	6.34	19.8	
> AL	8	9.64	E-02	D	.100	6.03	19.9	End 1st cycle
> 1/3	8	9.77	E-02	D	.100	5.05	20.2	~ T + 20.0 min
> CR	8	9.77	E-02	D	.100	5.05	20.2	← End Sweep 1

TABLE XXXII. COMPUTER PRINTOUT OF TEST NO. CPO-9

ID0	IDENTIFICATION		
	#LINES	5	
ID1	SINE TEST		
	MIL-STD 810B FIG. 514.1-4 CURVE (AR) 5HZ-20HZ AT .1DA		
ID2	TEST DESCRIPTION LINE 1		
	20HZ-2000HZ AT 2G'S TOTAL TEST TIME 2HRS. LESS 30MIN.		
ID3	TEST DESCRIPTION LINE 2		
	DWELL AT 10HZ		
ID4	DATE		
	OCT 5, 1973		
ID5	PREPARED BY		
	D.R.BRYANT		
IS0	INPUT SIGNALS		
	#LINES	1	
	XDUCER TYPE A,V,D	A	
IS1	ACCEL. SENS.		100
	MUX PORT		0
	AVERAGE	N	
	LEVEL RATIO		1
	SELECT-LO	N	
	SELECT-HI	Y	
	DISPLAY	Y	
	TRACK	Y	
FR0	FREQUENCIES		
	#LINES	4	
FR1	F LOW	5	
FR2	F HIGH	2000	

TABLE XXXII. COMPUTER PRINTOUT OF TEST NO. CPO-9 (CONT'D)

```
            FR3        F START        5

            FR4        F START INCREASING Y

            AP0        AMPLITUDE PROFILE
                       #LINES         2

            AP1        AMPL         9.99 E-02
                       A,V,D        D
                       INPUT F      N
                       F              5
                       ALARM           .919
                       ABORT          3

            AP2        AMPL           2
                       A,V,D        A
                       INPUT F      Y
                       F             20
                       ALARM           .919
                       ABORT          3

            TD0        TEST DURATION
                       #LINES         1

            TD1        TIME         Y
                       TIME          90
                       SWP CYCLES             Y
                       N              4.5
                       SWP SPD      N
                       SPEED           .862
                       SPECIMEN Q
                       L,M,H        L
>                                                          T+0
CR   8 9.79  E-02   D       .100      5.03       60.6   Test CPO-9 (Begin 4th cycle
>                                                                  at 5 Hz)
1/3  8        .101  D       .100      5.55       60.8
>
1/3  8        .102  D       .100      6.32       61.1
>
1/3  8        .102  D       .100      8.02       61.5
>
1/3  8        .101  D       .100     10.0        62
>
1/3  8        .101  D       .100     12.7        62.2
>
1/3  8        .101  D       .100     16          62.6
>
CR   8        .101  D       .100     19.9        63.1
>
1/3  8       2.01   A      2         21.2        63.1
>
1/3  8       2.01   A      2         25.4        63.5
>
1/3  8       2.01   A      2         32.1        63.9
>
1/3  8       2      A      2         40.4        64.2
>
1/3  8       2      A      2         50.9        64.5
>
```

TABLE XXXII. COMPUTER PRINTOUT OF TEST NO. CPO-9 (CONT'D)

1/3	8	2.02	A	2	64.2	65
>						
1/3	8	2	A	2	80.8	65.5
>						
1/3	8	2	A	2	102	65.8
>						
1/3	8	1.98	A	2	128	66
>						
1/3	8	2	A	2	162	66.7
>						
1/3	8	2	A	2	204	67
>						
1/3	8	2	A	2	257	67.5
>						
1/3	8	2	A	2	323	67.7
>						
1/3	8	2	A	2	408	68
>						
1/3	8	2	A	2	513	68.5
>						
1/3	8	2	A	2	647	68.8
>						
1/3	8	2	A	2	816	69.5
>						
1/3	8	2	A	2	1020	69.5
>						
1/3	8	2	A	2	1290	70
>						
1/3	8	2	A	2	1630	70.2
>						
CR	8	2	A	2	2000	70.8
>						
1/3	8	2	A	2	1620	71.3
>						
1/3	8	2	A	2	1280	71.5
>						
1/3	8	2	A	2	1020	72
>						
1/3	8	2	A	2	810	72.2
>						
1/3	8	2	A	2	642	72.5
>						
1/3	8	1.99	A	2	510	73
>						
1/3	8	2	A	2	405	73.3
>						
1/3	8	2	A	2	321	74
>						
1/3	8	1.95	A	2	255	74
>						
1/3	8	1.99	A	2	203	74.7
>						
1/3	8	2	A	2	161	75
>						
1/3	8	2	A	2	127	75.5
>						
1/3	8	2	A	2	101	75.8
>						

TABLE XXXII. COMPUTER PRINTOUT OF TEST NO. CPO-9 (CONT'D)

```
1/3 8      2        A     2         80.4      76.3
>
1/3 8      1.97     A     2         63.8      76.5
>
1/3 8      2        A     2         50.7      77.2
>
1/3 8      2        A     2         40.2      77.2
>
1/3 8      1.98     A     2         31.9      77.5
>
1/3 8      2        A     2         25.3      78.3
>
1/3 8      2        A     2         20.1      78.5
>
CR  8      1.99     A     2         20.0      78.5
>
1/3 8 9.96 E-02     D       .100    16        79
>
1/3 8 9.91 E-02     D       .100    12.7      79.2
>
1/3 8 9.89 E-02     D       .100    10.0      79.7
>
1/3 8 9.94 E-02     D       .100     8        80.2
>
1/3 8 9.77 E-02     D       .100     6.38     80.5
>
1/3 8 9.84 E-02     D       .100     5.04     80.8
```

End 4th cycle
T+20 min

TABLE XXXIII. COMPUTER PRINTOUT OF TEST NO. CPO-17

```
ID0       IDENTIFICATION
          #LINES          5

ID1       SINE TEST
          MIL-STD -167, 4-15HZ AT .030DA, 16-25HZ AT .020DA,26-33HZ

ID2       TEST DESCRIPTION LINE 1
          AT .010,34-40HZ AT .005HZ, 41-50HZ AT .003DA, VIB. AT

ID3       TEST DESCRIPTION LINE 2
          EVERY 1HZ INCREMENT FOR A 5MIN. DURATION.

ID4       DATE
          DWELL AT 7.5HZ,21HZ,42HZ, FOR  1HR . EA .10/19/73

ID5       PREPARED BY
          D.R. BRYANT

IS0       INPUT SIGNALS
          #LINES          1

          XDUCER TYPE  A,V,D  A
```

TABLE XXXIII. COMPUTER PRINTOUT OF TEST NO. CPO-17 (CONT'D)

```
IS1      ACCEL. SENS.            100
         MUX PORT                  0
         AVERAGE              N
         LEVEL RATIO               1
         SELECT-LO            N
         SELECT-HI            Y
         DISPLAY              Y
         TRACK                Y

FR0      FREQUENCIES
         #LINES          4

FR1      F LOW           4

FR2      F HIGH         50

FR3      F START         4

FR4      F START INCREASING Y

AP0      AMPLITUDE PROFILE
         #LINES          5

AP1      AMPL        3.00 E-02
         A, V, D     D
         INPUT F     N
         F               4
         ALARM            .919
         ABORT           3

AP2      AMPL        2.00 E-02
         A, V, D     D
         INPUT F     Y
         F              16
         ALARM            .919
         ABORT           3

AP3      AMPL        9.98 E-03
         A, V, D     D
         INPUT F     Y
         F              26
         ALARM            .919
         ABORT           3

AP4      AMPL        5.00 E-03
         A, V, D     D
         INPUT F     Y
         F              34
         ALARM            .919
         ABORT           3

AP5      AMPL        3.00 E-03
         A, V, D     D
         INPUT F     Y
         F              41
         ALARM            .919
         ABORT           3
```

TABLE XXXIII. COMPUTER PRINTOUT OF TEST NO. CPO-17 (CONT'D)

```
TD0      TEST DURATION
         #LINES        1

TD1      TIME      Y
         TIME          60
         SWP CYCLES          Y
         N             10
         SWP SPD   N
         SPEED          1.215
         SPECIMEN 0
         L,M,H     L

UP  8 2.94 E-02  D 3.00 E-02    4        0
>

AL  8 2.71 E-02  D 3.00 E-02    4        1.98
>

AL  8 3.17 E-02  D 3.00 E-02    4        3.67
>

AL  8 3.21 E-02  D 3.00 E-02    4        5.02
>

UP  8 2.36 E-02  D 3.00 E-02    5        0

AL  8 3.13 E-02  D 3.00 E-02    5        1.75
>

AL  8 2.75 E-02  D 3.00 E-02    5        3.45
>

AL  8 2.33 E-02  D 3.00 E-02    5        5.02
>

UP  8 3.02 E-02  D 3.00 E-02    6        0

PR  8 3.00 E-02  D 3.00 E-02    6        3.8
>PR

PR  8 2.93 E-02  D 3.00 E-02    6        4.39

AR 8 2.95 E-02  D 3.00 E-02     6        5.11

UP  8 3.02 E-02  D 3.00 E-02    7        0
```

TABLE XXXIII. COMPUTER PRINTOUT OF TEST NO. CPO-17 (CONT'D)

PR	8	2.98	E-02	D	3.00	E-02	7	3.57
PR	8	2.98	E-02	D	3.00	E-02	7	3.8
AB	8	2.98	E-02	D	3.00	E-02		5.11
UP	8	2.98	E-02	D	3.00	E-02	8	0
PR	8	2.99	E-02	D	3.00	E-02	8	1.20
PR	8	3.01	E-02	D	3.00	E-02	8	3.34
AB	8	2.98	E-02	D	3.00	E-02	8	5.09
UP	8	2.99	E-02	D	3.00	E-02	9	0
PR	8	2.99	E-02	D	3.00	E-02	9	1.75
PR	8	3.01	E-02	D	3.00	E-02	9	2.06
AB	8	2.99	E-02	D	3.00	E-02	9	5.09
UP	8	3.03	E-02	D	3.00	E-02	10	0
PR	8	3.01	E-02	D	3.00	E-02	10	2.60
AB	8	3.00	E-02	D	3.00	E-02	10	5.09
UP	8	3.04	E-02	D	3.00	E-02	11	0
PR	8	3.00	E-02	D	3.00	E-02	11	3.83
AB	8	3.00	E-02	D	3.00	E-02	11	5.06

TABLE XXXIII. COMPUTER PRINTOUT OF TEST NO. CPO-17 (CONT'D)

UP	8	2.94 E-Ø2	D	3.ØØ E-Ø2	12	Ø
PR	8	3.Ø1 E-Ø2	D	3.ØØ E-Ø2	12	2.92
AB	8	2.99 E-Ø2	D	3.ØØ E-Ø2	12	5.Ø6
UP	8	2.98 E-Ø2	D	3.ØØ E-Ø2	13	Ø
PR	8	3.ØØ E-Ø2	D	3.ØØ E-Ø2	13	3.24
AB	8	3.ØØ E-Ø2	D	3.ØØ E-Ø2	13	5.11
UP	8	2.98 E-Ø2	D	3.ØØ E-Ø2	14	Ø
PR	8	3.ØØ E-Ø2	D	3.ØØ E-Ø2	14	2.45
AB	8	2.98 E-Ø2	D	3.ØØ E-Ø2	14	5.Ø6
UP	8	3.ØØ E-Ø2	D	3.ØØ E-Ø2	15	Ø
PR	8	2.98 E-Ø2	D	3.ØØ E-Ø2	15	2.94
AB	8	3.ØØ E-Ø2	D	3.ØØ E-Ø2	15	5.Ø5
UP	8	2.95 E-Ø2	D	3.ØØ E-Ø2	16	Ø
PR	8	3.ØØ E-Ø2	D	3.ØØ E-Ø2	16	3.34
AB	8	3.Ø1 E-Ø2	D	3.ØØ E-Ø2	16	5.Ø5
UP	8	1.93 E-Ø2	D	2.ØØ E-Ø2	17	Ø
PR	8	2.ØØ E-Ø2	D	2.ØØ E-Ø2	17	4.Ø5

TABLE XXXIII. COMPUTER PRINTOUT OF TEST NO. CPO-17 (CONT'D)

AR	8	2.00 E-02	D	2.00 E-02	17	5.31
UP	8	1.98 E-02	D	2.00 E-02	18	0
PR	8	2.00 E-02	D	2.00 E-02	18	3.75
AR	8	2.00 E-02	D	2.00 E-02	18	5.06
UP	8	1.92 E-02	D	2.00 E-02	19	0
PR	8	1.99 E-02	D	2.00 E-02	19	3.25
AR	8	2.00 E-02	D	2.00 E-02	19	5.05
UP	8	2.00 E-02	D	2.00 E-02	20	0
PR	8	2.00 E-02	D	2.00 E-02	20	2.2
AL	8	3.06 E-03	D	2.00 E-02	20	4.17
UP	8	2.00 E-02	D	2.00 E-02	21	0
PR	8	1.99 E-02	D	2.00 E-02	21	2.95
AR	8	1.99 E-02	D	2.00 E-02	21	5.06
UP	8	1.97 E-02	D	2.00 E-02	22	0
PR	8	2.00 E-02	D	2.00 E-02	22	1.85
AR	8	2.00 E-02	D	2.00 E-02	22	5.03
UP	8	1.97 E-02	D	2.00 E-02	23	0
PR	8	2.00 E-02	D	2.00 E-02	23	3.13
AR	8	1.99 E-02	D	2.00 E-02	23	5.03

TABLE XXXIII. COMPUTER PRINTOUT OF TEST NO. CPO-17 (CONT'D)

UP	R	2.01 E-02	D	2.00 E-02	24	0
PR	R	1.99 E-02	D	2.00 E-02	24	2.62
AR	R	2.00 E-02	D	2.00 E-02	24	5.02
UP	R	1.98 E-02	D	2.00 E-02	25	0
PR	R	2.00 E-02	D	2.00 E-02	25	1.5
AR	R	2.00 E-02	D	2.00 E-02	25	5.03
UP	R	1.99 E-02	D	2.00 E-02	26	0
PR	R	2.00 E-02	D	2.00 E-02	26	2.8
AR	R	2.00 E-02	D	2.00 E-02	26	5.03
UP	R	9.53 E-03	D	1.00 E-02	27	0
PR	R	1.00 E-02	D	1.00 E-02	27	1.77
AR	R	9.98 E-03	D	1.00 E-02	27	5.03
UP	R	9.98 E-03	D	1.00 E-02	28	0
PR	R	9.95 E-03	D	1.00 E-02	28	3.22
AR	R	9.95 E-03	D	1.00 E-02	28	5.45
UP	R	9.70 E-03	D	1.00 E-02	29	0
PR	R	1.00 E-02	D	1.00 E-02	29	2.28
AR	R	9.98 E-03	D	1.00 E-02	29	5.02
UP	R	9.86 E-03	D	1.00 E-02	30	0

TABLE XXXIII. COMPUTER PRINTOUT OF TEST NO. CPO-17 (CONT'D)

PR	R	1.00	E-02	D	1.00	E-02	30	1.12
AR	R	9.93	E-03	D	1.00	E-02	30	4.93
UP	R	1.00	E-02	D	1.00	E-02	31	0
PR	R	9.95	E-03	D	1.00	E-02	31	3.67
AR	R	1.00	E-02	D	1.00	E-02	31	5.05
UP	R	1.00	E-02	D	1.00	E-02	32	0
PR	R	1.00	E-02	D	1.00	E-02	32	2.19
AR	R	1.00	E-02	D	1.00	E-02	32	5.03
UP	R	1.00	E-02	D	1.00	E-02	33	0
PR	R	9.98	E-03	D	1.00	E-02	33	2.65
AR	R	9.93	E-03	D	1.00	E-02	33	5.02
UP	R	1.01	E-02	D	1.00	E-02	34	0
PR	R	1.00	E-02	D	1.00	E-02	34	1.77
AR	R	9.98	E-03	D	1.00	E-02	34	5.06
UP	R	5.13	E-03	D	5.00	E-03	35	0
PR	R	5.00	E-03	D	5.00	E-03	35	3.47
AR	R	5.00	E-03	D	5.00	E-03	35	5.14
UP	R	4.90	E-03	D	5.00	E-03	36	0
PR	R	5.00	E-03	D	5.00	E-03	36	2.84
AR	R	5.02	E-03	D	5.00	E-03	36	5.02
UP	R	5.14	E-03	D	5.00	E-03	37	0
PR	R	5.00	E-03	D	5.00	E-03	37	2.98

TABLE XXXIII. COMPUTER PRINTOUT OF TEST NO. CPO-17 (CONT'D)

AR	8 5.00 E-03	D 5.00 E-03	37	5.27
UP	8 5.14 E-03	D 5.00 E-03	38	0
PR	8 5.00 E-03	D 5.00 E-03	38	1.72
AR	8 5.00 E-03	D 5.00 E-03	38	5.05
UP	8 4.90 E-03	D 5.00 E-03	39	0
AL	8 4.70 E-03	D 5.00 E-03	39	2.62
AR	8 5.00 E-03	D 5.00 E-03	39	4.70
UP	8 4.97 E-03	D 5.00 E-03	40	0
PR	8 5.00 E-03	D 5.00 E-03	40	2.69
AR	8 5.00 E-03	D 5.00 E-03	40	5.09
UP	8 5.13 E-03	D 5.00 E-03	41	0
PR	8 5.00 E-03	D 5.00 E-03	41	3.38
AR	8 5.00 E-03	D 5.00 E-03	41	4.984
UP	8 2.91 E-03	D 2.99 E-03	42	0
PR	8 2.99 E-03	D 2.99 E-03	42	2.37
AR	8 2.98 E-03	D 2.99 E-03	42	5.05
UP	8 3.06 E-03	D 2.99 E-03	43	0
PR	8 2.98 E-03	D 2.99 E-03	43	2.09
AR	8 2.98 E-03	D 2.99 E-03	43	5.09
UP	8 2.96 E-03	D 2.99 E-03	44	0
PR	8 3.01 E-03	D 2.99 E-03	44	3.02
AR	8 2.98 E-03	D 2.99 E-03	44	5.03

TABLE XXXIII. COMPUTER PRINTOUT OF TEST NO. CPO-17 (CONT'D)

UP	8	3.Ø4 E-Ø3	D 2.99 E-Ø3	45	Ø
PR	8	2.99 E-Ø3	D 2.99 E-Ø3	45	1.98
AR	8	2.99 E-Ø3	D 2.99 E-Ø3	45	5.Ø2
UP	8	3.Ø1 E-Ø3	D 2.99 E-Ø3	46	Ø
PR	8	2.98 E-Ø3	D 2.99 E-Ø3	46	1.9
AR	8	2.98 E-Ø3	D 2.99 E-Ø3	46	4.94
UP	8	3.Ø6 E-Ø3	D 2.99 E-Ø3	47	Ø
PR	8	2.97 E-Ø3	D 2.99 E-Ø3	47	2.6Ø
AR	8	3.ØØ E-Ø3	D 2.99 E-Ø3	47	5.Ø2
UP	8	2.98 E-Ø3	D 2.99 E-Ø3	48	Ø
PR	8	3.ØØ E-Ø3	D 2.99 E-Ø3	48	1.73
AR	8	3.ØØ E-Ø3	D 2.99 E-Ø3	48	5.Ø5
UP	8	2.98 E-Ø3	D 2.99 E-Ø3	49	Ø
PR	8	2.98 E-Ø3	D 2.99 E-Ø3	49	1.79
AR	8	2.98 E-Ø3	D 2.99 E-Ø3	49	4.98
UP	8	3.ØØ E-Ø3	D 2.99 E-Ø3	5Ø	Ø
AR	8	2.99 E-Ø3	D 2.99 E-Ø3	5Ø	5.Ø2

TABLE XXXIV. COMPUTER PRINTOUT OF TEST NO. CPO-18

```
IDØ     IDENTIFICATION
        #LINES        5

ID1     SINE TEST
        MIL-STD-331, TABLE (I) TEST 104 ,  6ØH-5ØØ-6ØHZ A5G'S

ID2     TEST DESCRIPTION LINE 1
        SAME AS ABOVE
```

TABLE XXXIV. COMPUTER PRINTOUT OF TEST NO. CPO-18 (CONT'D)

```
ID3       TEST DESCRIPTION LINE 2
          SAME AS ABOVE

ID4       DATE
          OCT. 23, 1973

ID5       PREPARED BY
          D.R.BRYANT

IS0       INPUT SIGNALS
          #LINES         1

          XDUCER TYPE  A,V,D  A

IS1       ACCEL. SENS.           100
          MUX PORT                 0
          AVERAGE             N
          LEVEL RATIO              1
          SELECT-LO           N
          SELECT-HI           Y
          DISPLAY             Y
          TRACK               Y

FR0       FREQUENCIES
          #LINES         4

FR1       F LOW         60

FR2       F HIGH       500

FR3       F START       60

FR4       F START INCREASING Y

AP0       AMPLITUDE PROFILE
          #LINES         1

AP1       AMPL           5
          A,V,D     A
          INPUT F   N
          F             60
          ALARM          .919
          ABORT          3

TD0       TEST DURATION
          #LINES         1

TD1       TIME      Y
          TIME        280
          SWP CYCLES          Y
          N              14
          SWP SPD   N
          SPEED           .306
          SPECIMEN Q
          L,M,H     L
```

TABLE XXXIV. COMPUTER PRINTOUT OF TEST NO. CPO-18 (CONT'D)

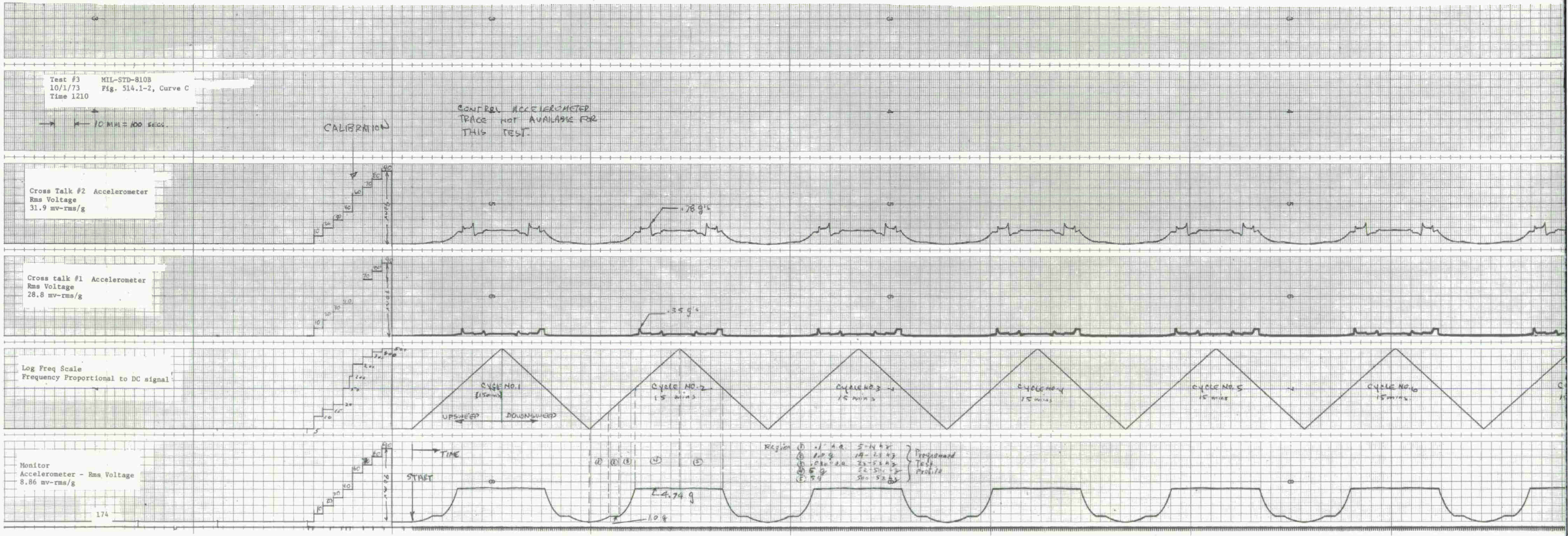
```
OK
>
TY  CH    LEVEL

UP   8     4.89    A     5       60         0
>
AL   8     4.55    A     5       61.7        .133
>
1/3  8     5.09    A     5       64          .301
>
1/3  8     5       A     5       80.6       1.42
>
1/3  8     5       A     5      101         2.53
>
1/3  8     4.98    A     5      128         3.64
>
1/3  8     4.98    A     5      161         4.73
>
1/3  8     5       A     5      203         5.86
>
1/3  8     5.02    A     5      256         6.95
>
1/3  8     5       A     5      323         8.03
>
1/3  8     5       A     5      407         9.16
>
CR   8     4.98    A     5      500        10.1
>
1/3  8     4.98    A     5      406        11.1
>
1/3  8     4.98    A     5      322        12.2
>
1/3  8     4.94    A     5      256        13.3
>
1/3  8     4.98    A     5      203        14.5
>
1/3  8     4.98    A     5      161        15.6
>
1/3  8     4.98    A     5      128        16.7
>
1/3  8     5       A     5      101        17.7
>
1/3  8     4.98    A     5       80.4      18.9
>
1/3  8     4.97    A     5       63.9      20.1
>
CR   8     4.98    A     5       60        20.2
>

ID0       IDENTIFICATION
          #LINES         5

ID1       SINE TEST
          MIL-STD 331, TABLE 1, TEST 104, 10-60-10HZ AT .1 DA.

ID2       TEST DESCRIPTION LINE 1
          OR 2G'S WHICH EVER IS LESSER
```

TABLE XXXIV. COMPUTER PRINTOUT OF TEST NO. CPO-18 (CONT'D)

```
ID3        TEST DESCRIPTION LINE 2
           SAME AS ABOVE

ID4        DATE
           OCT 24, 1973

ID5        PREPARED BY
           D.R. BRYANT

ISØ        INPUT SIGNALS
           #LINES          1

           XDUCER TYPE  A,V,D  A

IS1        ACCEL. SENS.             100
           MUX PORT                   Ø
           AVERAGE              N
           LEVEL RATIO                1
           SELECT-LO            N
           SELECT-HI            Y
           DISPLAY              Y
           TRACK                Y

FRØ        FREQUENCIES
           #LINES          4

FR1        F LOW           1Ø

FR2        F HIGH          6Ø

FR3        F START         1Ø

FR4        F START INCREASING Y

APØ        AMPLITUDE PROFILE
           #LINES          3

AP1        AMPL        9.99 E-Ø2
           A,V,D       D
           INPUT F     N
           F               1Ø
           ALARM            .919
           ABORT           3

AP2        AMPL            2
           A,V,D       A
           INPUT F     N
           F               19.78
           ALARM            .919
           ABORT           3

AP3        AMPL            2
           A,V,D       A
           INPUT F     Y
           F               6Ø
           ALARM            .919
           ABORT           3
```

TABLE XXXIV. COMPUTER PRINTOUT OF TEST NO. CPO-18 (CONT'D)

```
TD0       TEST DURATION
          #LINES          1

TD1       TIME       Y
          TIME           200
          SWP CYCLES              Y
          N               10
          SWP SPD    N
          SPEED              .250
          SPECIMEN 0
          L,M,H      L
>
TY  CH   LEVEL   AVD REFERENCE  FREQ-HZ  MIN
>
UP   8 9.91 E-02  D      .100    10         0
>
1/3  8 9.99 E-02  D      .100    10.1       0
>
1/3  8      .100  D      .100    12.7       1.37
>
1/3  8      .100  D      .100    16         2.69
>
CR   8      .100  D      .100    19.7       3.88
>
1/3  8     2      A     2        20.1       4
>
1/3  8     2      A     2        25.4       5.36
>
1/3  8     2.02   A     2        32.0       6.67
>
1/3  8     2      A     2        40.3       7.98
>
1/3  8     2      A     2        50.8       9.31
>
CR   8     2      A     2        59.9      10.2
>
CR   8     2      A     2        59.9      10.2
>
1/3  8     2      A     2        50.7      11.2
>
1/3  8     2      A     2        40.2      12.5
>
1/3  8     2      A     2        32        13.8
>
1/3  8     2      A     2        25.4      15.2
>
1/3  8     2.01   A     2        20.1      16.5
>
CR   8     2      A     2        19.8      16.6
>
1/3  8 9.99 E-02  D      .100    16        17.7
>
1/3  8 9.96 E-02  D      .100    12.7      19.1
>
1/3  8      .100  D      .100    10.0      20.4
>
CR   8 9.96 E-02  D      .100    10        20.4
```



Test #3
10/1/73
Time 1210
MIL-STD-810B
Fig. 514.1-2, Curve C
10 MM = 100 SECS.
CALIBRATION
CONTROL ACCELEROMETER TRACE NOT AVAILABLE FOR THIS TEST.
Cross Talk #2 Accelerometer
Rms Voltage
31.9 mv-rms/g
.78 g's
Cross talk #1 Accelerometer
Rms Voltage
28.8 mv-rms/g
.35 g's
Log Freq Scale
Frequency Proportional to DC signal
CYCLE NO. 1
UPSWEEP
DOWNSWEEP
CYCLE NO. 2
15 mins
CYCLE NO. 3
15 mins
CYCLE NO. 4
15 mins
CYCLE NO. 5
15 mins
CYCLE NO. 6
15 mins
Monitor
Accelerometer - Rms Voltage
8.86 mv-rms/g
TIME
START
4.74 g
1.0 g
174

a

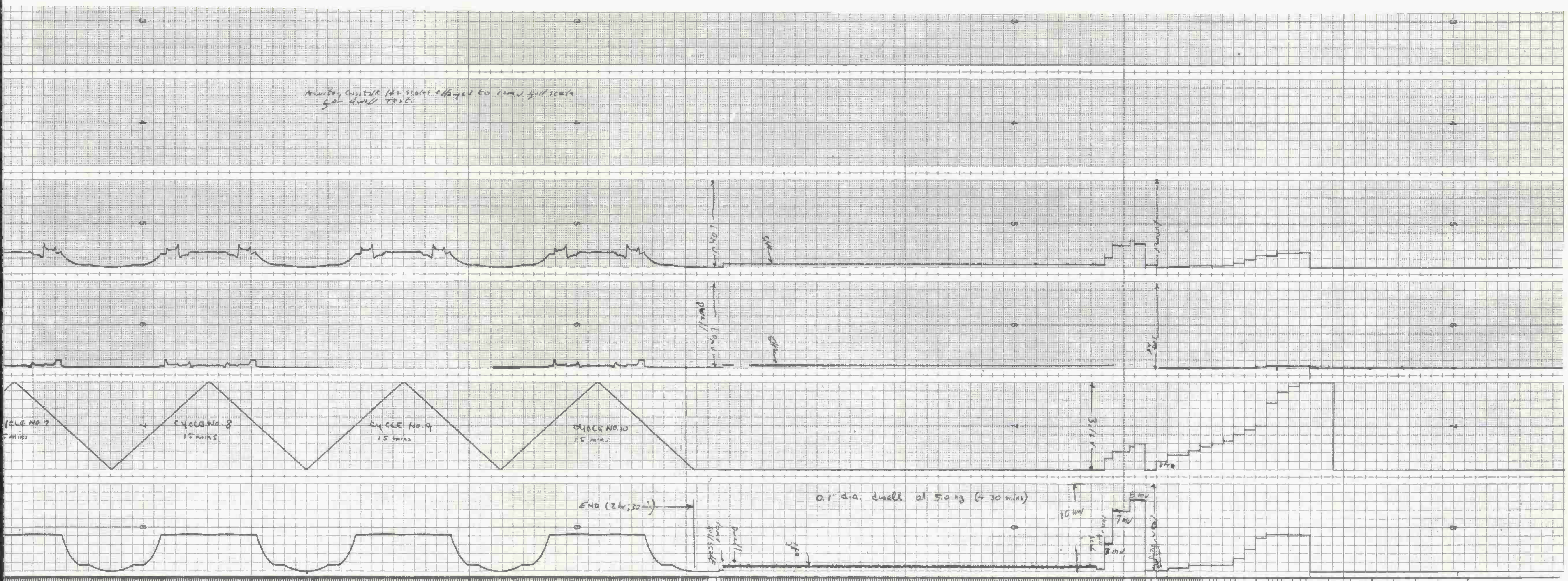
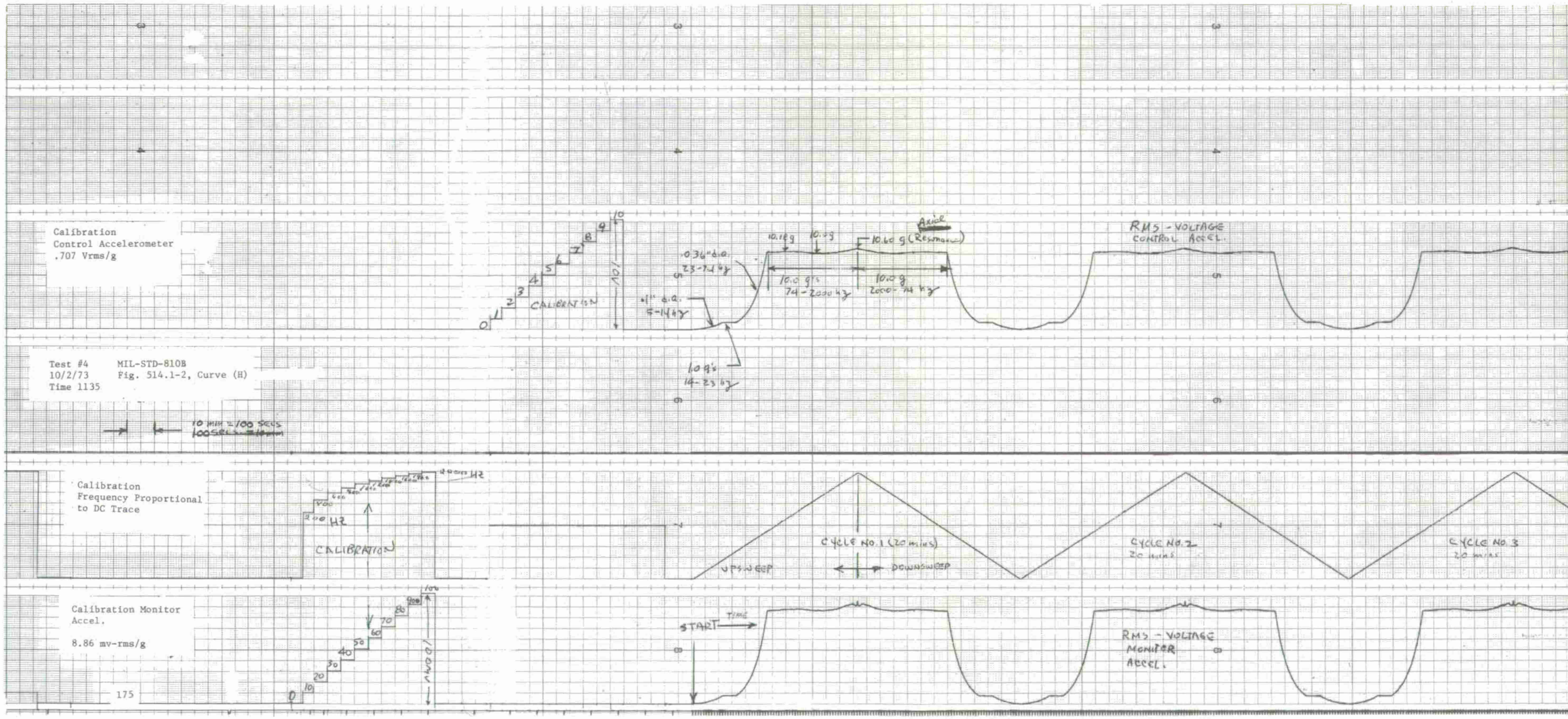


Figure 39. Analog strip-chart data for test No. 3.


Calibration
Control Accelerometer
.707 Vrms/g
CALIBRATION
RMS - VOLTAGE
CONTROL ACCEL.
Test #4 MIL-STD-810B
10/2/73 Fig. 514.1-2, Curve (H)
Time 1135
Calibration
Frequency Proportional
to DC Trace
CALIBRATION
UPSWEEP
CYCLE NO. 1 (20 mins)
DOWNSWEEP
CYCLE NO. 2
20 mins
CYCLE NO. 3
20 mins
Calibration Monitor
Accel.
8.86 mv-rms/g
175
START
TIME
RMS - VOLTAGE
MONITOR
ACCEL.

a

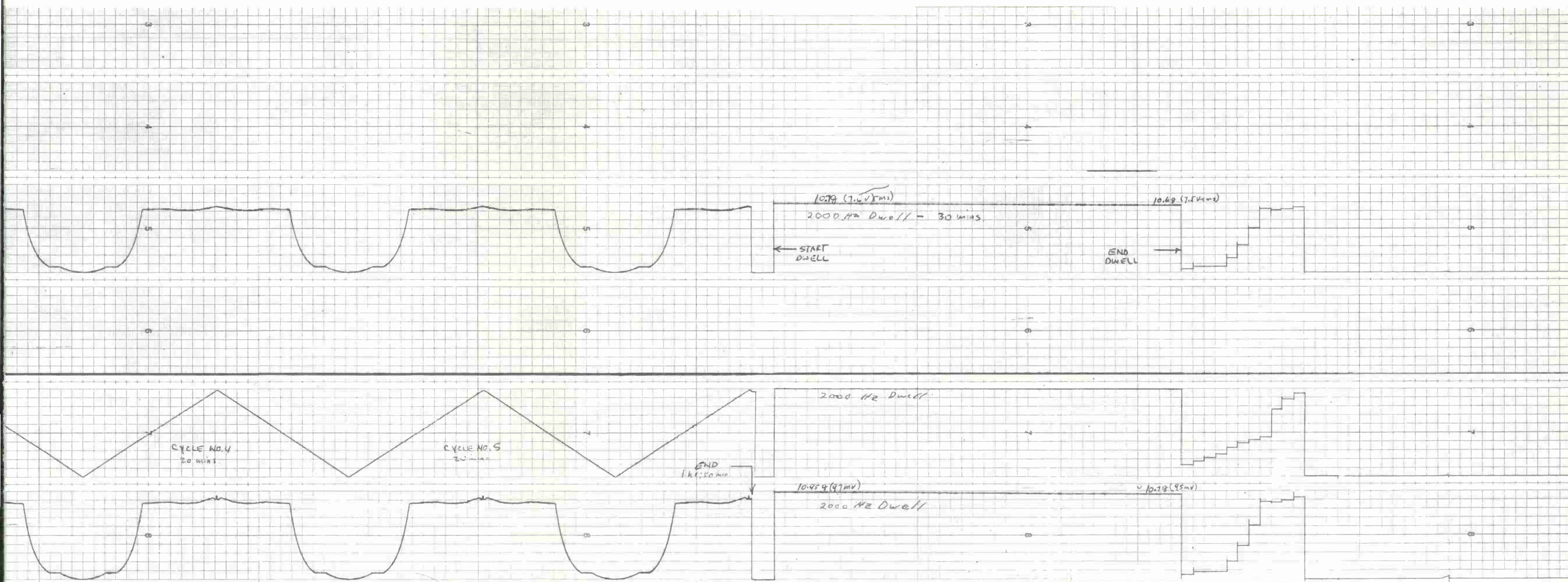
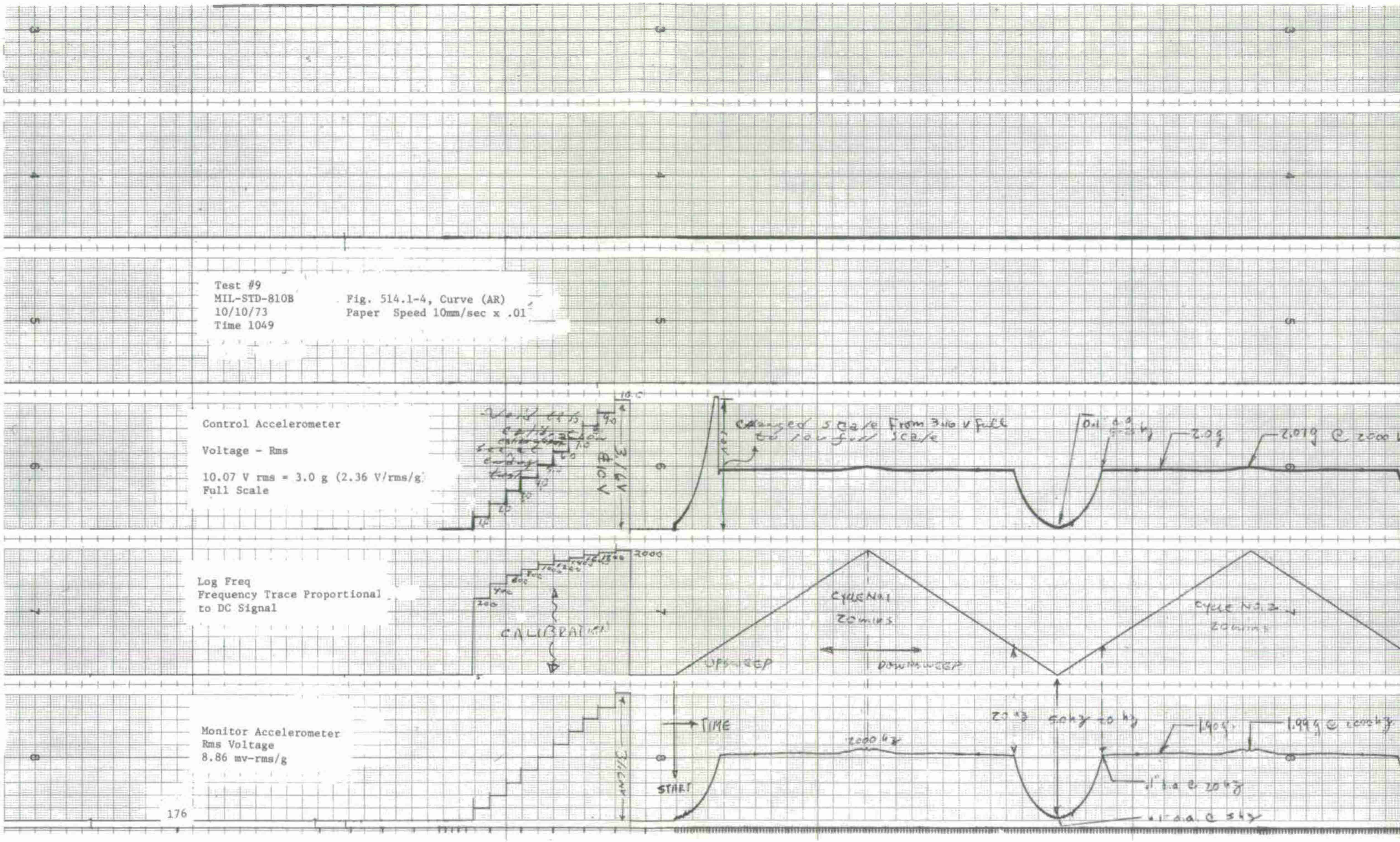


Figure 40. Analog strip-chart data for test No. 4.

b


Test #9
MIL-STD-810B
10/10/73
Time 1049
Fig. 514.1-4, Curve (AR)
Paper Speed 10mm/sec x .01
Control Accelerometer
Voltage - Rms
10.07 V rms = 3.0 g (2.36 V/rms/g)
Full Scale
Log Freq
Frequency Trace Proportional
to DC Signal
Monitor Accelerometer
Rms Voltage
8.86 mv-rms/g
CALIBRATION
UPSWEEP
DOWNSWEEP
TIME
START
2000
2000 hz
2.0 g

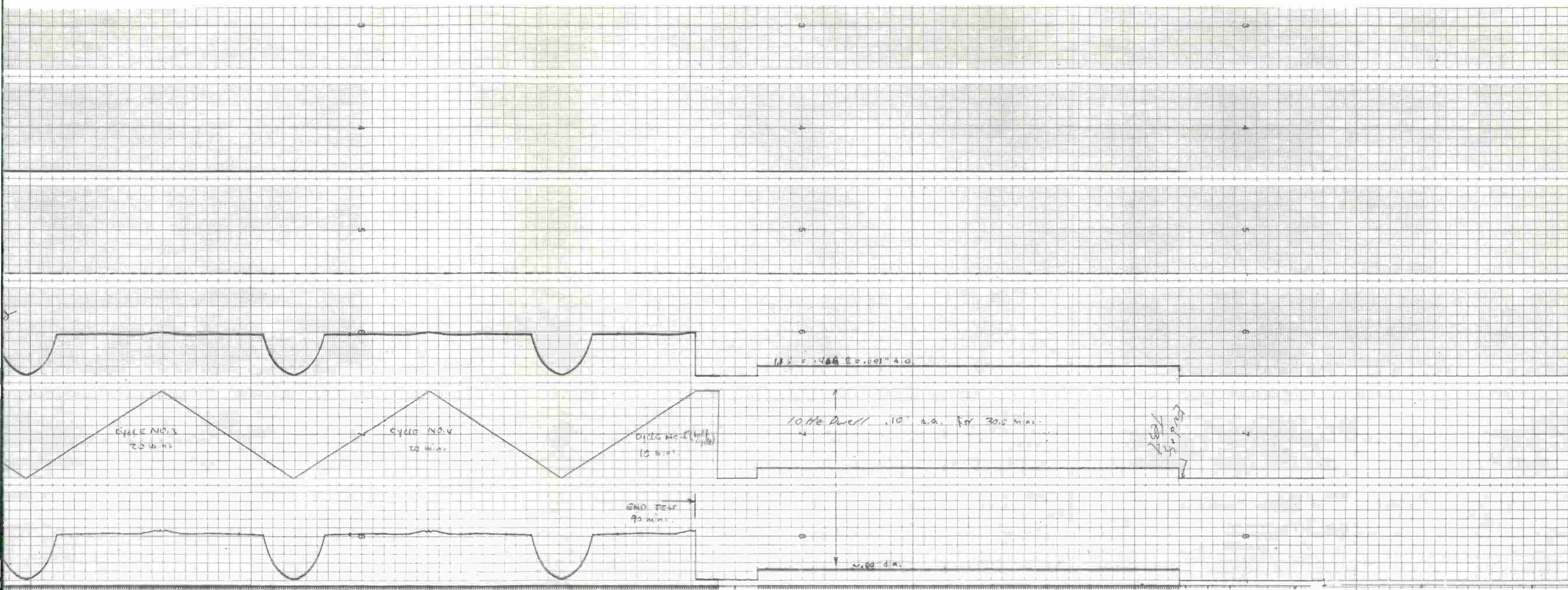


Figure 41. Analog strip-chart data for test No. 9.

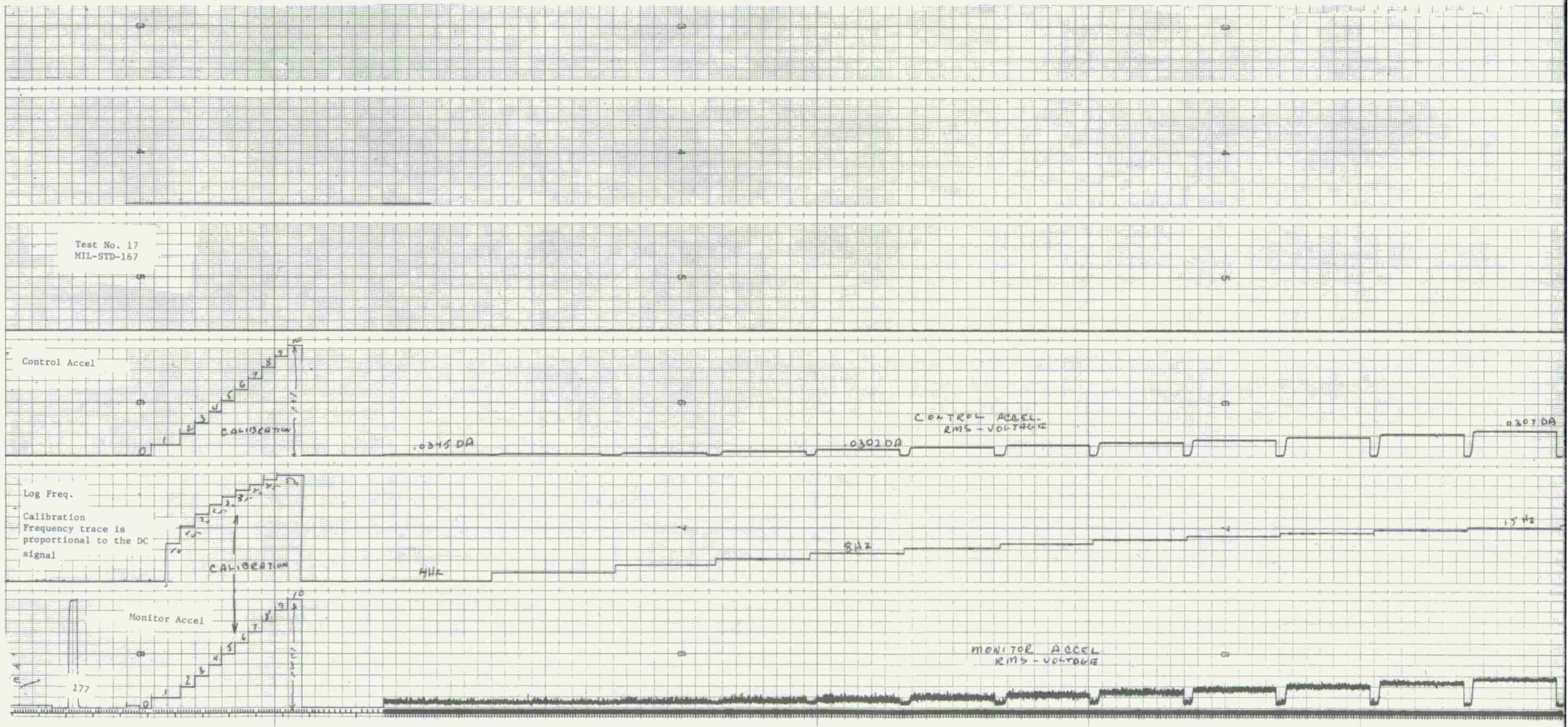
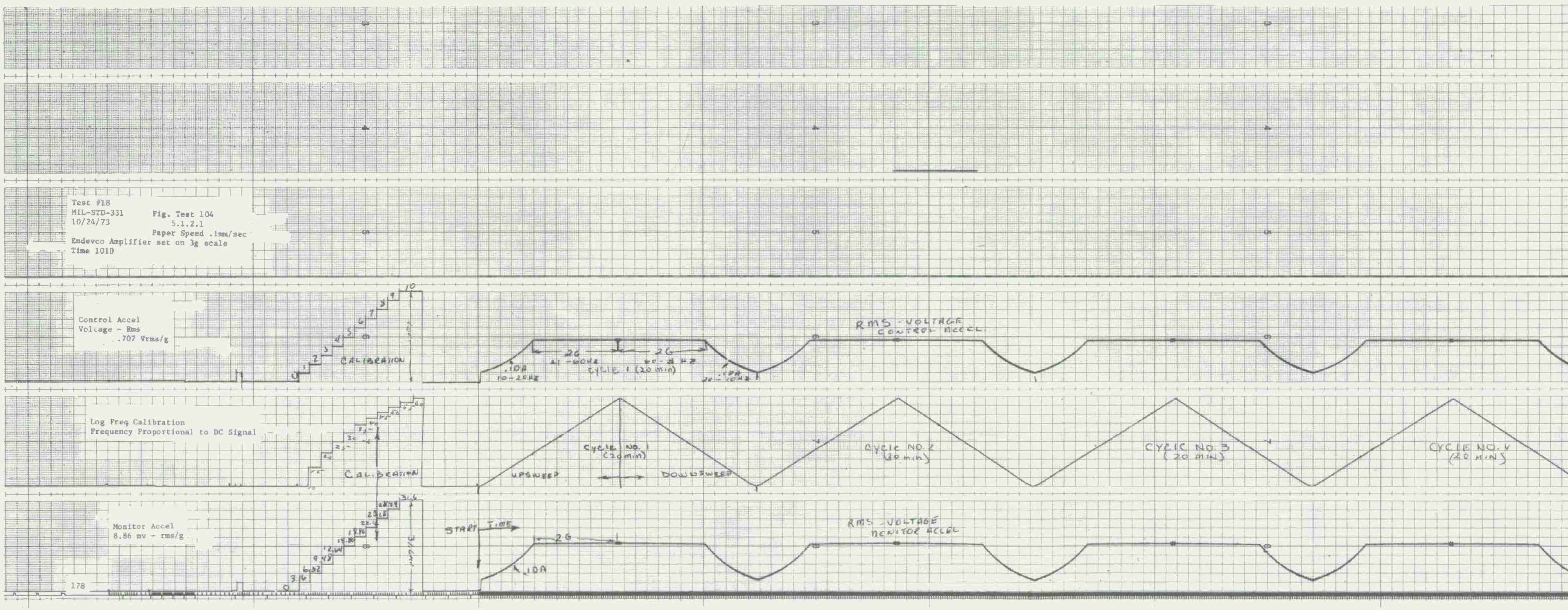

Test No. 17
MIL-STD-167
Control Accel
CALIBRATION
.0345 DA
.0302 DA
CONTROL ACCEL
RMS - VOLTAGE
.0307 DA
Log Freq.
Calibration
Frequency trace is
proportional to the DC
signal
CALIBRATION
4Hz
8Hz
15 Hz
Monitor Accel
MONITOR ACCEL
RMS - VOLTAGE
177
a

Figure 42. Analog strip-chart data for test No. 17.

b



Test #18
MIL-STD-331
10/24/73
Fig. Test 104
5.1.2.1
Paper Speed .1mm/sec
Endevco Amplifier set on 3g scale
Time 1010
Control Accel
Voltage - Rms
.707 Vrms/g
CALIBRATION
RMS - VOLTAGE
CONTROL ACCEL
CYCLE 1 (20 min)
Log Freq Calibration
Frequency Proportional to DC Signal
CALIBRATION
UPSWEEP
DOWNSWEEP
Cycle NO. 1
(20 min)
CYCLE NO. 2
(20 min)
CYCLE NO. 3
(20 MIN)
CYCLE NO. 4
(20 MIN)
Monitor Accel
8.86 mv - rms/g
START TIME
RMS - VOLTAGE
MONITOR ACCEL
178

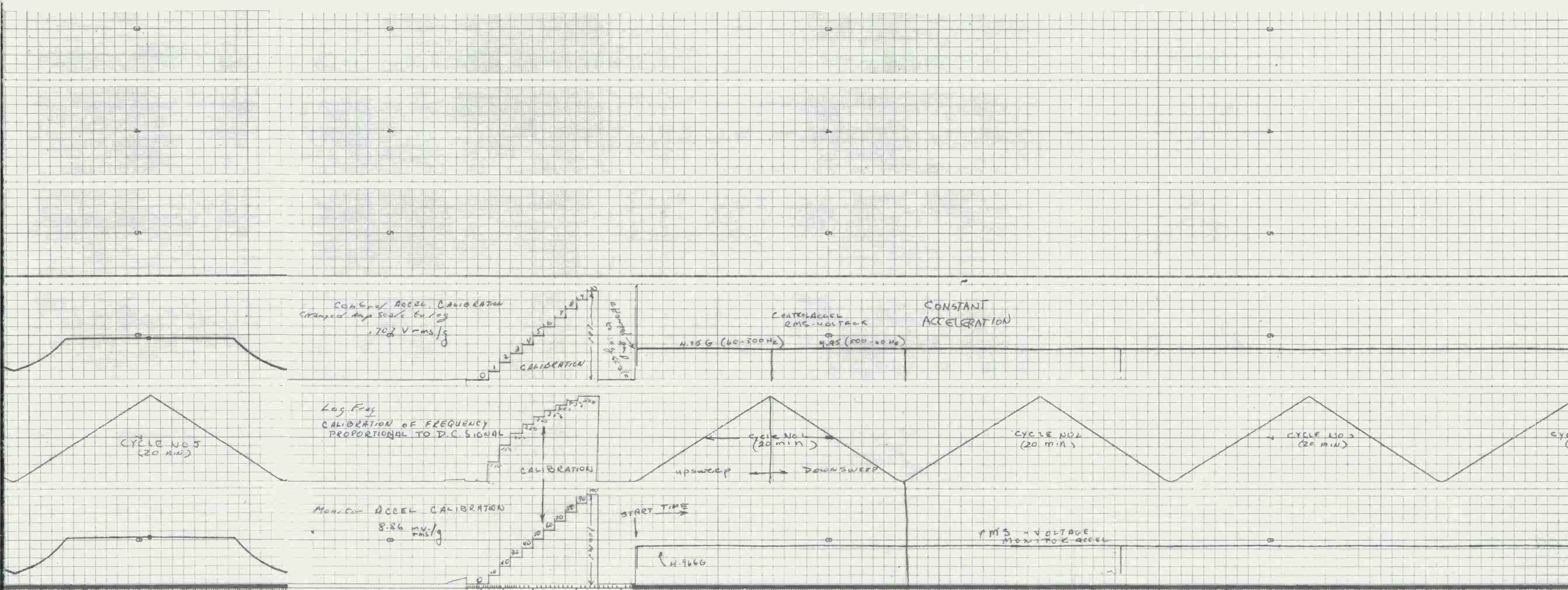


Figure 43. Analog strip-chart data for test No. 18.

Voltage points can be selected at particular frequencies to confirm the accuracy of the readings against the computer-indicated results for the known transducer sensitivity. Although the strip recorder has a ±1.0-dB frequency response, analog data were analyzed for amplitude accuracy and found to be well within ±10 percent of the specified values listed in the computer printout. (This was confirmed for all tests.)

10.3.3 Photographic Data of Digitally Synthesized Sinusoidal Input

Photographic data depicting the input voltage and frequency to the exciter driving power amplifier, as well as the exciter response voltage and frequency, are presented in figures 44 through 47 for the indicated tests. The input voltage is computer controlled by the precision gain amplifier, whereas the driving waveform is synthesized by the digital oscillator. The dynamic response of the exciter is recorded by the control accelerometer whose output voltage and frequency is monitored by the computer/oscillator control loop. The two traces were photographed at the same time while operating in the dwell mode. The top trace (T) designates the input signal, whereas the bottom trace (B) represents the feedback signal from the control accelerometer.

Clearly evident is the significant harmonic distortion of the exciter in the band of 5 to 28 Hz. This distortion, however, is characteristic of the dynamic response of this exciter/load combination at low frequency, and would exist regardless of whether the control system were analog or digital in nature. The harmonic distortion is certainly not caused by the digital oscillator, as even at low frequencies the input signal is observed to be practically distortion free. (Also contributing to the harmonic distortion is the ever present 60-Hz noise superimposed on the signal.) Not related to the concept of digital control testing technique is the phase angle (estimated at 50 to 70 deg) between the input and output signals.

Regarding the digital control, we conclude that a smooth, practically distortion-free drive signal can be synthesized by the digital oscillator, at least within the frequency band of 5 to 2000 Hz. Distortion tests performed on this (bare) exciter with a HP distortion analyzer indicate maximum distortion of 3 percent around 20 Hz at the center of the table. The driving signal is synthesized from 32 voltage steps polarity inverted quoter sine cycle.

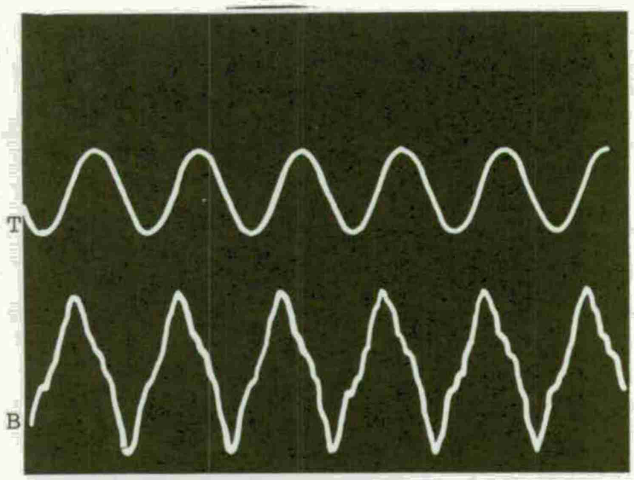
10.4 Resonance Search and Dwell Tests and Data Obtained

Among the prime objectives in military sine-sweep vibration tests is the objective to determine the resonant frequency within the specified test band. Once this frequency is determined, a 20- to 30-min dwell test is typically required per specifications MIL-STD-810B and -331. Another primary objective of this test program was to demonstrate direct-digital control of any dwell test that might be encountered within these specifications. Specific test frequencies were selected to simulate resonance dwell in the 5- to 2000-Hz band for the test specified in the

Test No. 15

.75 in. (D.A.) Dwell at 5.5 Hz

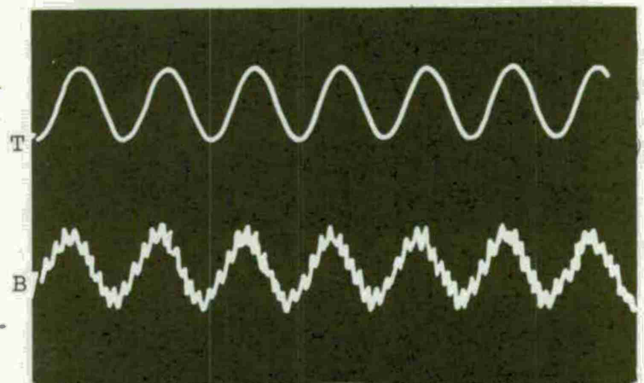
Top Trace	Bottom Trace
Input to exciter	Output of control accelerometer
5 V/cm	1 V/cm (10 V F.S. = *)
.1 sec/cm	.1 sec/cm



Test No. 1

.1 in. (D.A.) Dwell at 6.5 Hz

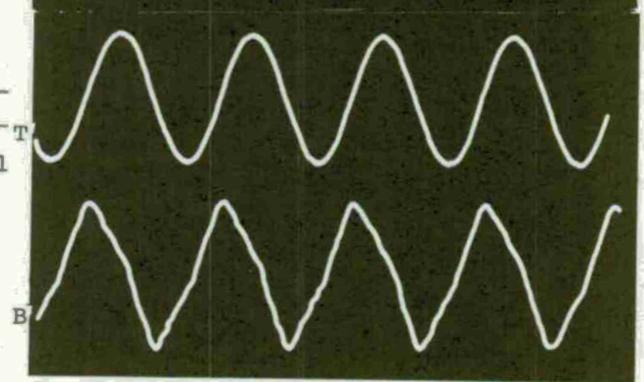
Top Trace	Bottom Trace
Input to exciter	Output of control accelerometer
1 V/cm	2 V/cm (10 V F.S. = *)
.1 sec/cm	.1/cm



Test No. 14

.75 in. (D.A.) Dwell at 8.5 Hz

Top Trace	Bottom Trace
Input to exciter	Output of control accelerometer
5 V/cm	1 V/cm
.050 sec/cm	(10 V F.S. = *) .050 sec/cm



*10 volts full scale is related to peak amplitude as follows:

0 ≤ peak amplitude ≤ 1.0 g, full scale 1.0 g
1.0 g ≤ (" ") ≤ 3.0 g, full scale = 3.0 g
30 g ≤ (" ") ≤ 10.0 g, full scale = 10.0 g
10 g ≤ (" ") ≤ 30.0 g, full scale = 30.0 g
30 g ≤ (" ") ≤ 100 g, full scale = 100.0 g

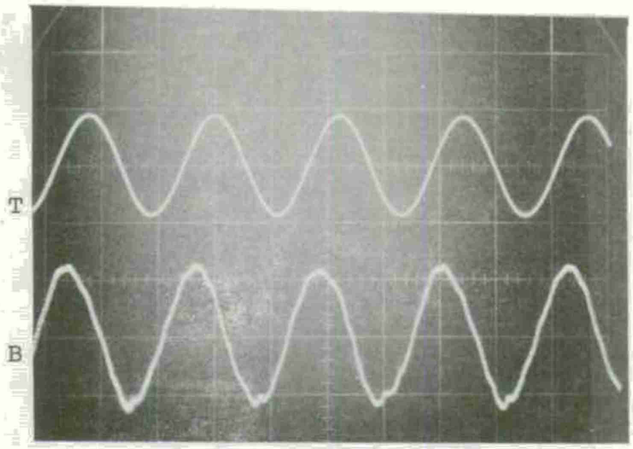
Figure 44. Selected digitally synthesized sinusoidal input data for tests 15, 1, and 14.

(all curves were traced from original data)

Test No. 9

1 in. (D.A.) Dwell at 10 Hz

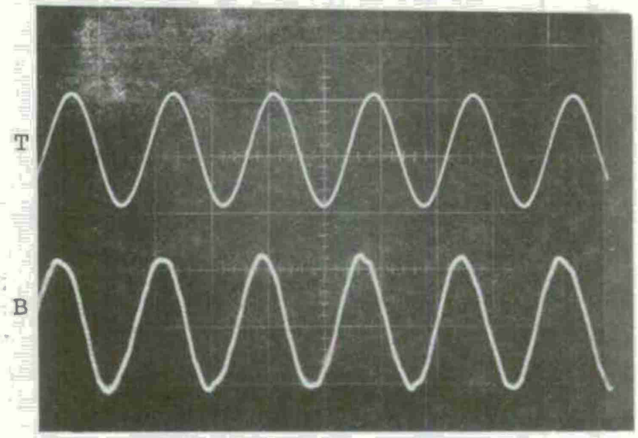
Top Trace	Bottom Trace
Input to exciter	Output of control accelerometer
1 V/cm	1 V/cm
.050 sec/cm	(10 V F.S. = *) .050 sec/cm



Test No. 8

1.0 g   Dwell at 22.5 Hz

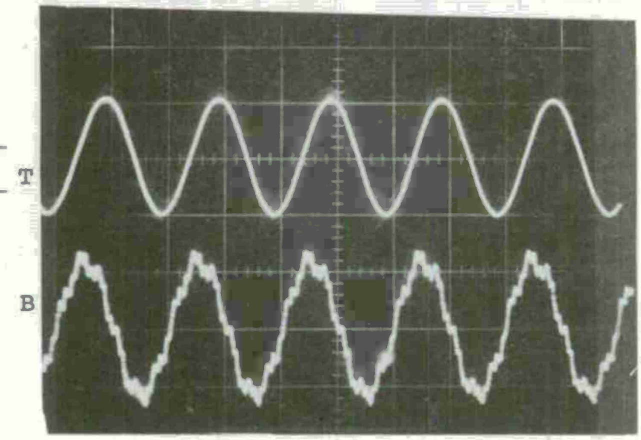
Top Trace	Bottom Trace
Input to exciter	Output of control accelerometer
1.0 V/cm	1.0 V/cm
.020 sec/cm	(10 V F.S. = *) .020 cm



Test No. 16

.036 in. (D.A.) Dwell at 28.0 Hz

Top Trace	Bottom Trace
Input to exciter	Output of control accelerometer
1.0 V/cm	1.0 V/cm
.020 sec/cm	(10 V F.S. = *) .020 sec/cm



*10 volts full scale is related to peak amplitude as follows:

$0 \leq$ **peak amplitude** ≤ 1.0 g, full scale 1.0 g
1.0 g $\leq$ ("   "   ) $\leq$ 3.0 g, full scale = 3.0 g
30 g $\leq$ ("   "   ) $\leq$ 10.0 g, full scale = 10.0 g
10 g $\leq$ ("   "   ) $\leq$ 30.0 g, full scale = 30.0 g
30 g $\leq$ ("   "   ) $\leq$ 100 g, full scale = 100.0 g

Figure 45. Selected digitally synthesized sinusoidal input data for tests 9, 8, and 16.

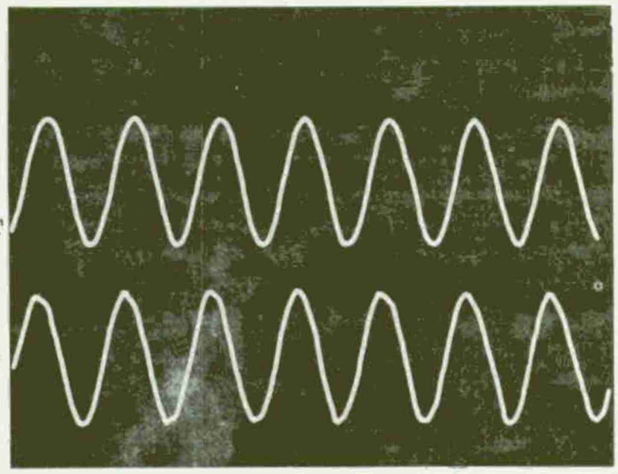
(all curves were traced from original data)

Test No. 6

.036 in. (D.A.) Dwell at 33.0 Hz

Top Trace	Bottom Trace
Input to exciter	Output of control accelerometer
1.0 V/cm	1.0 V/cm
.020 sec/cm	(10 V F.S. = *) .020 sec/cm

T
B

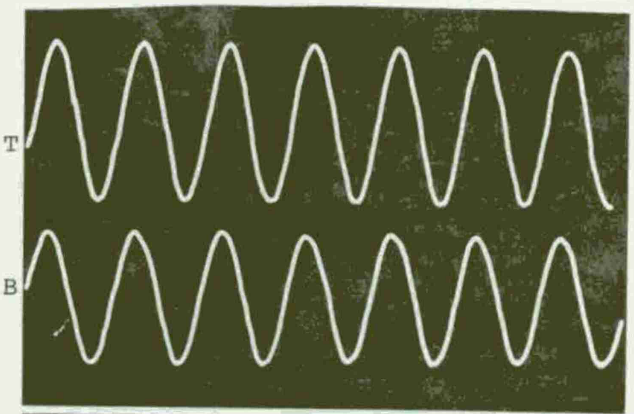


Test No. 6

2.0 g Dwell at 66.0 Hz

Top Trace	Bottom Trace
Input to exciter	Output of control accelerometer
1.0 V/cm	1.0 V/cm
.010 sec/cm	(10 V F.S. = *) .010/cm

T
B

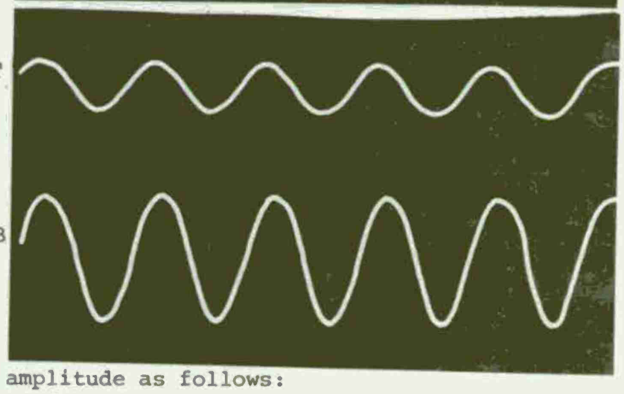


Test No. 7

5.0 g Dwell at 250.0 Hz

Top Trace	Bottom Trace
Input to exciter	Output of control accelerometer
1 V/cm	1.0 V/cm
2/m sec/cm	(10 V F.S. = *) 2/m sec/cm

T
B



*10 volts full scale is related to peak amplitude as follows:

$0 \leq$ peak amplitude $\leq$ 1.0 g, full scale 1.0 g
1.0 g $\leq$ (" ") $\leq$ 3.0 g, full scale = 3.0 g
30 g $\leq$ (" ") $\leq$ 10.0 g, full scale = 10.0 g
10 g $\leq$ (" ") $\leq$ 30.0 g, full scale = 30.0 g
30 g $\leq$ (" ") $\leq$ 100 g, full scale = 100.0 g

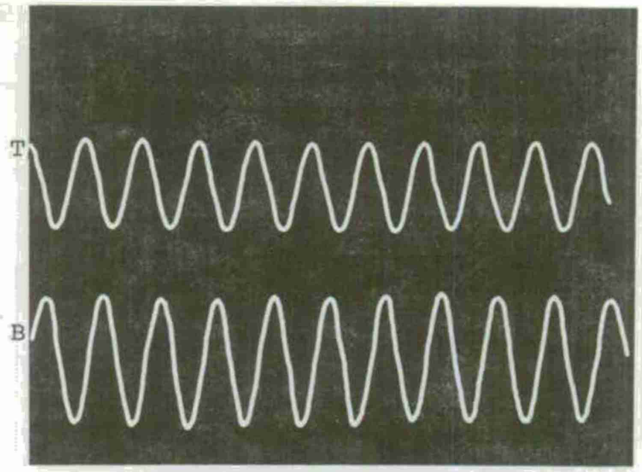
Figure 46. Selected digitally synthesized sinusoidal input data for tests 6 and 7.

(all curves were traced from original data)

Test No. 13

1.5 g Dwell at 500.0 Hz

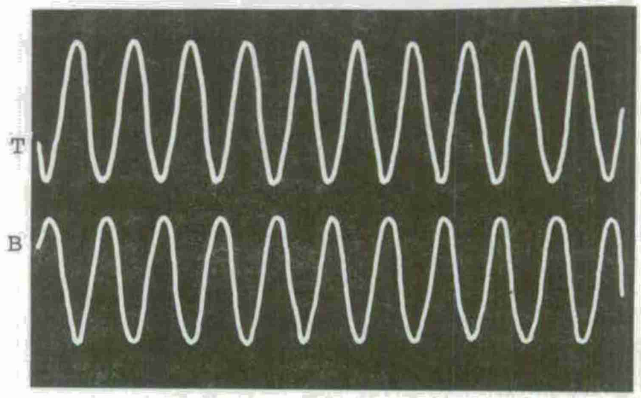
Top Trace	Bottom Trace
Input to exciter	Output of control accelerometer
.2 V/cm	1 V/cm
	(10 V F.S. = *)
2 m sec/cm	2 msec/cm



Test No. 4

10.0 g Dwell at 2000 Hz

Top Trace	Bottom Trace
Input to exciter	Output of control accelerometer
1.0 V/cm	1.0 V/cm
	(10 V F.S. = *)
.5 msec/cm	.5 msec/cm



*10 volts full scale is related to peak amplitude as follows:

0 ≤ peak amplitude ≤ 1.0 g, full scale 1.0 g
1.0 g ≤ (" ") ≤ 3.0 g, full scale = 3.0 g
30 g ≤ (" ") ≤ 10.0 g, full scale = 10.0 g
10 g ≤ (" ") ≤ 30.0 g, full scale = 30.0 g
30 g ≤ (" ") ≤ 100 g, full scale = 100.0 g

Figure 47. Selected digitally synthesized sinusoidal input data for tests 13 and 4.

(all curves were traced from original data)

test matrix (see sect 9.1). A significant number of these dwell frequencies was selected at regions for which direct-digital control might be particularly difficult to implement. This included dwell at 5.0 or 2000 Hz (lower/upper limits, respectively), a dwell at the exact acceleration to displacement crossover frequency, a dwell at half-frequency point such as 8.5 Hz, or a dwell at maximum system displacement limits (0.75 in. D. A.). The remaining dwell frequencies were selected arbitrarily to simulate random resonance condition. The result here is to execute a wide variety of sine-dwell tests covering the entire spectrum of cases expected. Note that since the test article was not actually resonating at the selected frequencies, these tests only demonstrate "simulated" resonance (except at 2000 Hz as described below). The primary demonstrations sought during the simulated resonance/dwell tests were:

(a) Digital control of any arbitrary test amplitude outlined in the specifications MIL-STD-810B and -331.

(b) Steady-amplitude control to within the ±10-percent envelope over the required 20- to 30-min dwell derive (that is, demonstrate that any drift is within ±10 percent of the specified test amplitude).

(c) Check out the amplitude compensation feature of the DDC test system, by which excessive amplitude magnifications during resonance can be automatically compensated for through inverse transfer function techniques, causing the gain to be compressed to within ±10 percent of the specified amplitude. (The actual control capabilities at any frequency will depend, of course, on the particular load/exciter dynamics.)

Once a test frequency was selected from a (simulated) dwell case, the test was executed in the identical manner stipulated in specifications MIL-STD-810B and -331. (This applies also to the simulated dwell for amphibious equipment per MIL-STD-167.) One might argue that a simulated dwell test, where resonance does not actually exist, is fundamentally different from resonance test where dynamic interactions could result in loss of amplitude control. But the primary consideration here was to evaluate the adequacy of the direct-digital-control technique during the extended dwell operation. It so happened that at 2000-Hz maximum load/exciter resonance was observed.

Review of both analog (strip-chart) data (figs. 39-43) and the digital printout data for all dwell tests (tables XXIX-XXXIII) indicate all test amplitudes were maintained well within the ±10-percent control requirement. No significant drifts were observed; when they did materialize occasionally, the ±10-percent amplitude control requirement was still maintained. Voltage traces for both monitor and control accelerometers indicated smooth and steady response throughout the dwell tests, in effect confirming each other's output. Of particular interest, however, was amplitude control at 2000 Hz where maximum load/exciter resonance was observed on analog data. Manufacturer's data state the bare table

resonance to be 4.3:1 at this frequency.* Our test data confirm resonance buildup starting at approximately 1300 Hz and peaking at 2000 Hz. This is evident from strip-chart data for test No. 4 (MIL-STD-810B - 514.2-2, curve H) presented in section 10.3. Data for the 10 g, 30.0-min dwell at 2000 Hz obtained from the two accelerometers are given as follows:

	Begin dwell (T+0 min)	End dwell (T+30 min)
Control accelerometer (DVM)	10.70 g (+7.0%)	10.60 (+6.0%)
Monitor accelerometer (DVM)	10.95 g (+9.5%)	10.61 g (+6.1%)

Noted here is that the control accelerometer maintained amplitude control to within 7 ±1 percent in contrast to the non-resonance cases where amplitude control can be limited to well within 5 ±1 percent (see tables VII-XXVII, sect 10.1).

The increased loss of control is undoubtedly due to the resonance effects. The fact that the monitor accelerometer indicated a larger error (compared with the control accelerometer--that is, +9.5 percent versus +7.0 percent) is due to the fact that this measurement is not in close proximity to the control accelerometer. Its physical location (90-deg clockwise from the control measurement but on same 3.0-in. diameter), as well as many other points on the fixture, will experience larger excitation during resonance than would the control station, simply because only one location is used for control. It is the control input that the DDC test system attempts to regulate; this has been successfully demonstrated to within the required ±10 percent, using the automatic compensation feature. This by no means suggests that direct-digital control could be automatically used for any resonance tests, as a variety of dynamic conditions exist for which neither the conventional analog nor the new direct-digital control system could comply with the ±10-percent control requirement. It merely suggests compliance with statements (a), (b), and (c) stated in this section and leads to the conclusion that the direct-digital control test could be safely incorporated into military resonance dwell testing per specifications MIL-STD-810B and -331.

Computer printouts for most of the tested dwell-modes are presented in tables XXXIV through XXXXV (column interpretation is identical with the procedure outlined in sect 10.3.2, table XXIX). A review of these data quickly affirms compliance with the ±10-percent amplitude control

---

**C-90 exciter typical bare table axial resonance data:*

2000 Hz - 4.3:1
2500 Hz - 12.9:1

requirement for the indicated fixed frequency. Time listings of each amplitude is obtained by taking the arithmetic average ($\bar{M}$) of n samples taken within 1/2-2.0 sec prior to, and including, the indicated time:

$$\bar{M} = \sqrt{\sum_{i=1}^{i=n} \frac{Mi^2}{i}}$$

[where M^2 represents the squared value of instantaneous amplitudes]

The index n is optimized against the test frequency and sweep rate, and is based on a sample rate (SR) of $64 \leq SR \leq 5/2$ samples/sec.

10.5 Test Amplitude Repeatability and Voltage Drift Effects

The reliability of the DDC test system was investigated for all tests specified in the test matrix (table IV). This investigation seeks to demonstrate that the DDC test system can accurately repeat and control the programmed test profile over as many sweep cycles and sweep rates as specified.

Analog data from the two accelerometers were reviewed for all tests. The results indicate excellent repeatability between two sweep cycles anywhere in the test, regardless of sweep speed or excitation mode. This is clearly evident from analog data presented in section 10.1. A simple technique used to confirm repeatability consisted of tracing the rms voltage of the first (or second) test cycle on transparent paper, and overlaying this trace on as many sweep cycles as desired. It quickly becomes apparent that the sweep cycles are, in fact, mirror images of each other—a trend confirmed for both control and monitor accelerometers. Based on this technique, it was concluded that errors due to cycle-to-cycle repeatability are practically nonexistent. A backup tecnnique was then adopted by which the analog rms voltage data from the monitor accelerometer were converted into the equivalent vibration mode at all programmable end points and center points. For example, given a test profile of .1 in. D.A. 5 to 14 Hz, 1.0 g 14 to 23 Hz, 0.036 in. D.A. 23 to 52 Hz (ref test No. 3), rms voltage data would be obtained from analog record at 5, 10, 14, 18, 23, 38, 52 Hz etc., and converted into the appropriate displacement/acceleration mode at the indicated frequency. Since the data were plotted on a log scale, a trace having a zero slope (constant voltage) would designate constant acceleration, whereas a trace indicating a positive or negative slope would designate constant displacement mode, as the rms voltage is proportional to the quantity (XW^2) of the overall driving signal - $V = (XW^2) \sin wt$. (Note that up-sweep and down-sweep displacement result in positive and negative slopes respectively.) Each analog trace was analyzed according to this procedure and the results compared with the numerical value of the programmed test amplitude (available from digital data). These calculations confirmed that the programmed amplitudes and test

measured amplitudes were well within ±10 percent of each other for any two sweep cycles compared. In fact, most deviations centered around 5 ± 1 percent.

Since any 3 points are sufficient to define a well-behaved curve, voltage traces can be checked for amplitude drifts with sweep frequency. For displacement modes, this is achieved by demonstrating that any three points lie on a curve defined mathematically by the amplitude quantity (XW^2).* Constant acceleration modes on the other hand yield straight line of zero slope (constant voltage), as the rms voltage is proportional to g(rms) of the acceleration-drive signal. Review of the analog rms voltage data indicated that any three arbitrary points, for any particular vibration mode, coincided well with the calculated accelerometer voltage data for that vibration mode. Furthermore, this trend was maintained for as many sweep cycles as tested. Therefore, amplitude drift effects as functions of sweep frequency can be discounted with confidence.

10.6 Test Program Setup Time - Production/Qualification Testing

Table XXXXVI contains a summary of the time required to prepare all necessary program tapes to perform the tests specified in the test matrix (table IV). The specific times listed for each function tape are subsequently added to yield total pretest setup time. The indicated time values apply only to the preparation of the required functional tapes; time expanded in installing the fixture/specimen assembly is not listed here, as it is unique for specific assemblies.

The time data presented herein pertain to the specific read-type punch hardware and state of optimization of software associated with this (T5021) DDC test system. Faster printers or tape readers will, of course, reduce the overall setup time. The required setup time will also depend on the operator's skill and experience. These data serve merely as a guide, indicating typical orders of magnitude of the effort involved. Such data would be of particular interest to organizations engaged in military production/qualification testings.

Three different total setup times are presented in columns 6, 7, and 8 of table XXXXVI. Column 6 is obtained by a straightforward addition of all the preceding columns. It indicates the total pretest setup time required to execute the specified test, with no initial preparation whatsoever. These data show the average total setup time to be 17.75 min. If, on the other hand, all applicable test tapes had been retained from previous test work, times specified in columns 1, 2, and 3 would be automatically eliminated, yielding an average total setup time of 4.15 min, or 77 percent improvement over the cold start case. The total setup time can be further reduced by storing all functional program tapes on a permanent record such as a

---

**Given the square-law-voltage buildup with frequency, if any point does not coincide with the indicated analog voltage trace, the only conclusion that can be drawn here is that amplitude drift exists.*

disc system (limited to a 32,000-word-core capacity for PDP-11/20 computer). The only setup time required, then, would be the transfer of appropriate information from storage into the computer—a high-speed loading process that can be accomplished well under 1 min. Once the appropriate test tapes have been programmed (17.75 min), use of the last technique will practically eliminate the setup time for subsequent tests. Furthermore, this technique maximizes test reliability, as human intervention and therefore human errors are kept to a minimum. The 1-min total setup time represents a 76-percent improvement over the present setup time (4.15 min) required for repeated testing, and 95-percent improvement compared with the cold start case.

The total setup times involved in disc storage test operation are presented in column 8 of table XXXXVI. Unlike the rest of the data, figures for this column were carefully *estimated*, based on the state of software and loading rate of the computer. Future developments at this facility call for disc storage of all the tests performed herein, at which time actual data will become available.

The procedure outlining the specific functional and data tapes required to perform a direct-digitally controlled test is presented in section 4.1. The time data included here present a step-by-step breakdown of this pretest setup procedure.

The obvious trend that is demonstrated by the various data on total test setup times is the speed with which the standard Army sine-sweep vibration tests can be programmed, coupled with increased test reliability, and reduced cost. Recent software developments permit a single operator to simultaneously command several sine* tests, relying only on a pushbutton series of conversational instructions—an improvement that is bound to reduce overhead expenses.

Data presented in column 1 indicate the net listing time only, whereas data in column 2 pertain to the total time required to *EDIT* and *LIST* the data tape. Occasionally, it is observed that a two-level sine test required a longer *edit* and *list* period than did, say, a three-level test. This is due to the fact that debugging operations involved in the initial preparation of the tapes are not always related to the number of programmable steps.

10.7 Summary of Acceptance Tests

A series of acceptance tests was performed throughout the last quarter of FY 73 and midway into the first half of the first quarter of FY 74 to determine the DDC test system performance under a variety of max/min/nominal conditions. Also, the acceptance test series was intended to shake down the control/exciter system, ascertain the

---

**Several exciters can be driven simultaneously by a single control system.*

dynamic response of a loaded exciter, and check out the adequacy of the sine-sweep software. Successful completion of these objectives would have released the DDC test system to perform the military standard sine-sweep vibration tests specified in the test matrix. In addition to the max/min/nominal tests, extremely low-level long-duration sine-sweep tests were also attempted. A summary of the acceptance tests program is presented in table XXXXVII for sweep rates varying between 0.1 and 7.0 octaves/min, within the frequency band of 5 to 3000 Hz. The required ABORT limit was ±1.0 dB (approx ±10-percent amplitude control), and maximum sustained acceleration level attempted was 120.0 g.

Review of the acceptance tests data indicates the following:

(1) All test profiles programmed were successfully executed. Low-level tests (below 1.0 g) in the frequency range of 5 to 15 Hz were aborted occasionally due to excessive system noise. High-level tests (exceeding 100 g) were controlled to within ±1.0 dB despite the fact that significant resonance buildup developed around 3000 Hz. (Bare table axial resonance at 3000 Hz exceeds 20:1.)

(2) Trimming and calibration of the signal conditioning units (D701/D710) were required to avoid premature saturation at high-level tests, as full range is limited to 5.0 V.

(3) State of software was adequate, except that no provisions were made to retain feedback amplitude and frequency information at sweep speeds exceeding maximum real-time printout rate (approx 3.0 octaves/min). As a result, test documentation for sweep speeds between 3.0 and 7.0 octaves/min was not possible, as these data were lost. However, a backup data source exists in the form of the digitized amplitude voltage versus frequency plot for the entire test envelope.

(4) The DDC test system demonstrated its ability to operate within vibration environments far in excess of those demanded by the standard Army specifications such as MIL-STD-810B, -331, -167 and others. Particularly, acceleration levels as high as 120 g were generated, controlled, and maintained. Amplitude step changes of 100:1 and 1000:1 were successfully attempted, indicating a dynamic-range capability as high as 60 dB. Also successfully demonstrated were 10 levels mixed acceleration, velocity, displacement sine-sweep programs at cycling rates between 0.1 and 7.0 octaves/min, within the frequency band of 5 to 3000 Hz.

TABLE XXXV. DWELL TEST NO. 1

This portion of the test was dwell at 11 Hz for a duration of 30 min.

1	2	3	4	5	6	7
UP	8	.100	D	.100	11	0
>PR						
PR	8	.100	D	.100	11	.969
>PR						
PR	8	.100	D	.100	11	3.45
>PR						
PR	8	9.99 E-02	D	.100	11	7.70
>PR						
PR	8	.100	D	.100	11	11.8
>PR						
PR	8	9.96 E-02	D	.100	11	16.3
>PR						
PR	8	.100	D	.100	11	16.4
>PR						
PR	8	.100	D	.100	11	18.3
>PR						
PR	8	.100	D	.100	11	19.4
>PR						
PR	8	.100	D	.100	11	19.6
>PR						
PR	8	.100	D	.100	11	21.1
>PR						
PR	8	9.99 E-02	D	.100	11	22.9
>PR						
PR	8	9.99 E-02	D	.100	11	23.8
>PR						
PR	8	.100	D	.100	11	24.6
>PR						
PR	8	9.99 E-02	D	.100	11	25.1
>PR						
PR	8	.100	D	.100	11	27.4
>PR						
PR	8	9.99 E-02	D	.100	11	29.2
>PR						
PR	8	9.99 E-02	D	.100	11	30.1
>						
MANUAL ABORT						
AB	8	.100	D	.100	11	30.2
>						

Column Definition
1 - PR≡Print
2 - Channel No. 8
3 - Test amplitude
4 - D≡Displacement("DA)
    A≡Acceleration (g)
5 - Test amplitude requested
6 - Frequency (Hz)
7 - Time (Min)

Note:
Printouts for dwell tests 4,8,9,19,21,22, 23, are not included herein.

TABLE XXXVI. DWELL TEST NO. 2

```
DWELL AT 500HZ FOR 30 MIN.

>FC 500

OK
>HO
>
UP  5    2    A    2    500    0
>PR

PR  5    2    A    2    500    .666
>PR

PR  5    2    A    2    500    13.5
>PR

PR  5    2    A    2    500    13.7
>PR

PR  5    2    A    2    500    14
>PR

PR  5    2    A    2    500    21.7
>PR

PR  5    2    A    2    500    21.9
>PR

PR  5    2    A    2    500    22
>PR

PR  5    2    A    2    500    22.1
>PR

PR  5    2    A    2    500    27.9
>PR

PR  5    2    A    2    500    28.1
>PR

PR  5    2    A    2    500    28.4
>PR

PR  5    2    A    2    500    29.2
>PR

PR  5    2    A    2    500    29.5
>PR

PR  5    2    A    2    500    29.6
>PR

PR  5    2    A    2    500    29.7
>PR

PR  5    2    A    2    500    30.1
>
*MANUAL ABORT*
AB 5    2    A    2    500    30.2
>
```

TABLE XXXVII. DWELL TEST NO. 3

Dwell at 5 Hz for 30 min

```
                  MAMA
PASSWORD:

OK
>FC 5

OK
>HO

>
UP   8 9.81 E-02   D      .100     5        0
>PR

PR   8      .100   D      .100     5        2.56
>PR

PR   8      .100   D      .100     5        2.73
>PR

PR   8 9.99 E-02   D      .100     5        5.69
>PR

PR   8 9.96 E-02   D      .100     5        7.83
>PR

PR   8 9.99 E-02   D      .100     5        8.19
>PR

PR   8      .100   D      .100     5       12.5
>PR

PR   8 9.99 E-02   D      .100     5       16.7
>PR

PR   8      .100   D      .100     5       19.4
>PR

PR   8 9.96 E-02   D      .100     5       23.2
>PR

PR   8 9.99 E-02   D      .100     5       26.5
>PR

PR   8      .100   D      .100     5       29.4
>PR

PR   8      .100   D      .100     5       29.6
>PR

PR   8      .100   D      .100     5       29.7
>PR

PR   8      .100   D      .100     5       30

>
*MANUAL ABORT*
AB 8 9.99 E-02  D      .100     5       30.1
>
```

TABLE XXXVIII. DWELL TEST NO. 4

```
                 DWELL 100HZ FOR  30MIN.
FC 100
OK
>HO
>
UP  8  3.70  E-02   D 3.59  E-02    100          0
>PR
PR  8  3.59  E-02   D 3.59  E-02    100          1.05
>PR
PR  8  3.59  E-02   D 3.59  E-02    100          2.82
>PR
PR  8  3.59  E-02   D 3.59  E-02    100          5.3
>PR
PR  8  3.60  E-02   D 3.59  E-02    100          7.14
>PR
PR  8  3.58  E-02   D 3.59  E-02    100         10.5
>PR
PR  8  3.59  E-02   D 3.59  E-02    100         10.7
>PR
PR  8  3.59  E-02   D 3.59  E-02    100         17.5
>PR
PR  8  3.59  E-02   D 3.59  E-02    100         17.6
>PR
PR  8  3.58  E-02   D 3.59  E-02    100         17.8
>PR
PR  8  3.58  E-02   D 3.59  E-02    100         18.9
>PR
PR  8  3.60  E-02   D 3.59  E-02    100         19.6
>PR
PR  8  3.58  E-02   D 3.59  E-02    100         22
>PL
?
>PR
PR  8  3.59  E-02   D 3.59  E-02    100         24.2
>PR
PR  8  3.59  E-02   D 3.59  E-02    100         26
>PR
PR  8  3.60  E-02   D 3.59  E-02    100         27.4
PRR 8  3.58  E-02   D 3.59  E-02    100         29.2
                    D 3.59  E-02    100         29.6
> PR
?
>PR
PR  8  3.59  E-02   D 3.59  E-02    100         29.8
>PR
PR  8  3.58  E-02   D 3.59  E-02    100         30
>
*MANUAL ABORT*
AB 8 3.58 E-02  D 3.59 E-02   100         30.1
>
```

TABLE XXXIX. DWELL TEST NO. 6

DWELL AT 33HZ AND 66HZ FOR 3ØMIN EA.

```
HO
>
UP  8     1.96    A    2     33     Ø
>PR
PR  8     2       A    2     33     2.75
>PR
PR  8     2       A    2     33     7.81
>PR
PR  8     2       A    2     33     13.8
>PR
PR  8     2       A    2     33     2Ø.1
>PR
PR  8     2       A    2     33     2Ø.2
>PR
PR  8     2       A    2     33     21.3
>PR
PR  8     2       A    2     33     26.5
>PR
PR  8     2       A    2     33     27.6
>PR
PR  8     2       A    2     33     27.8
>PR
PR  8     2       A    2     33     28.7
>PRPR
PR  8     2       A    2     33     29.7
>PR
PR  8     2       A    2     33     29.9
>PR
PR  8

*MANUAL ABORT*
AB 8      2       A    2     33     3Ø.1
>

FC 66
OK
>HO
>
UP  8     5.Ø8    A    5     66     Ø
>PR
PR  8     4.98    A    5     66     1.38
>PR
PR  8     4.97    A    5     66     3.91
>PR
PR  8     5       A    5     66     4.Ø5
>PR
```

TABLE XXXIX. DWELL TEST NO. 6 (CONT'D)

```
PR   8     4.98   A    5      66       8.59
>PR
PR   8     4.98   A    5      66       11.1
>PR
PR   8     5      A    5      66       12.8
>PR
PR   8     5      A    5      66       15.7
>PR
PR   8     4.98   A    5      66       18.9
>PR
PR   8     5.02   A    5      66       24
>PR
PR   8     5      A    5      66       25.3
>PR
PR   8     4.97   A    5      66       29.2
>PR
PR   8     4.98   A    5      66       29.7
>PR
PR   8     4.97   A    5      66       30
>
*MANUAL ABORT*
AR   8     5      A    5      66       30.1
>!A
>
```

TABLE XXXX. DWELL TEST NO. 7

DWELL AT 250HZ FOR 30 MIN

```
FC 250

OK
>HO
>
UP   8     5.33   A    5      250      0
>PR
PR   8     5      A    5      250      1.75
>PR
PR   8     5.02   A    5      250      3.32
>PR
PR   8     5.02   A    5      250      8.38
>PR
PR   8     4.98   A    5      250      13.6
>PR
PR   8     5      A    5      250      13.8
>PR
PR   8     4.98   A    5      250      19.4
>PR
```

TABLE XXXX. DWELL TEST NO. 7 (CONT'D)

```
PR  8     4.98    A     5       250        19.6
>PR

PR  8     5       A     5       250        22.2
>PR

PR  8     4.97    A     5       250        22.4
>PR

PR  8     4.98    A     5       250        25.4
>PR

PR  8     5       A     5       250        27.1
>PL
?
>PR

PR  8     4.97    A     5       250        28
>PR

PR  8     4.98    A     5       250        29.2
>PR

PR  8     5       A     5       250        29.5
>PR

PR  8     4.98    A     5       250        29.7
>PR

PR  8     5       A     5       250        30
>
*MANUAL ABORT*
AB 8     4.98    A     5       250        30
>
```

TABLE XXXXI. DWELL TEST NO. 13

Dwell at 500 Hz for 30 min

```
FC 500

OK
>40
>
UP  8     1.5     A     1.5     500         0
>PR

PR  8     1.5     A     1.5     500         .150
>PR

PR  8     1.5     A     1.5     500         5.73
>PR

PR  8     1.49    A     1.5     500         9.16
>PR

PR  8     1.5     A     1.5     500        10.7
>
?
>PR
```

TABLE XXXXI. DWELL TEST NO. 13 (CONT'D)

```
PR  8    1.5    A    1.5    500    12.7
>PR

PR  8    1.49   A    1.5    500    15.3
>PR

PR  8    1.5    A    1.5    500    18.3
>PR

PR  8    1.5    A    1.5    500    26.3
>PR

PR  8    1.49   A    1.5    500    26.5
>PR

PR  8    1.49   A    1.5    500    28.1
>PR

PR  8    1.5    A    1.5    500    28.6
>PR

PR  8    1.5    A    1.5    500    29.2
>PR

PR  8    1.5    A    1.5    500    30
>
*MANUAL ABORT*
AB 8    1.5    A    1.5    500    30.1
>
```

TABLE XXXXII. DWELL TEST NO. 14

Dwell at 8.5 Hz for 30 min

```
>
UP  8    .742   D    .75    8.5    0
>PR

PR  8    .75    D    .75    8.5    .25
>PR

PR  8    .748   D    .75    8.5    .434
>PR

PR  8    .748   D    .75    8.5    .617
>PR

PR  8    .75    D    .75    8.5    4.73
>PR

PR  8    .748   D    .75    8.5    6.41
>PR

PR  8    .75    D    .75    8.5    16.3
>PR
```

TABLE XXXXII. DWELL TEST NO. 14 (CONT'D)

```
PR  8        .75   D        .75        8.5        18.5
>PR

PR  8        .75   D        .75        8.5        20.2
>PR

PR  8        .748  D        .75        8.5        26.3
>PRPR

PR  8        .75   D        .75        8.5        29.8
>PR

PR  8        .748  D        .75        8.5        30
>
*MANUAL ABORT*
AB 8        .748  D        .75        8.5        30
>
```

TABLE XXXXIII. DWELL TEST NO. 15

Dwell at 5.5 Hz for 10 min

```
>
UP  8        .779  D        .75        5.5        0
>PR

PR  8        .75   D        .75        5.5         .133
>PR

PR  8        .75   D        .75        5.5        1.02
>PR

PR  8        .75   D        .75        5.5        1.99
>PR

PR  8        .75   D        .75        5.5        2.02
>PR

PR  8        .75   D        .75        5.5        2.13
>PR

PR  8        .748  D        .75        5.5        2.84
>PR

PR  8        .75   D        .75        5.5        3.65
>PR

PR  8        .75   D        .75        5.5        6.3
>PR

PR  8        .75   D        .75        5.5        7.93
>PR

PR  8        .746  D        .75        5.5        9.13
>PR
```

TABLE XXXXIII. DWELL TEST NO. 15 (CONT'D)

```
PR  8      .75    D      .75      5.5      9.25
>PR

PR  8      .746   D      .75      5.5      9.34
>PR

PR  8      .75    D      .75      5.5      10.0
>
*MANUAL ABORT*
AB 8      .748   D      .75      5.5      10.2
>
```

TABLE XXXXIV. DWELL TEST NO. 16

Dwell at 28 Hz for 10 min

```
>
UP  8      1.49   A      1.5      28       0
>PR

PR  8      1.5    A      1.5      28       .150
>PR

PR  8      1.5    A      1.5      28       2.92
>PRPR

PR  8      1.5    A      1.5      28       3.73
>PR

PR  8      1.5    A      1.5      28       4.28
>PR

PR  8      1.5    A      1.5      28       4.52
>PR

PR  8      1.5    A      1.5      28       5.03
>PR

PR  8      1.5    A      1.5      28       6.52
>PR

PR  8      1.5    A      1.5      28       8.03
>PR

PR  8      1.5    A      1.5      28       8.56
>PR

PR  8      1.5    A      1.5      28       10
>PR

PR  8      1.5    A      1.5      28

*MANUAL ABORT*
AB 8      1.5    A      1.5      28       11.1
>
```

TABLE XXXXV. DWELL TEST NO. 17

Dwell at 21 Hz for 1 hr.

```
FC 21

OK
>10
>
UP   8  2.01  E-02   D  2.00  E-02     21          0
>PR

PR   8  2.00  E-02   D  2.00  E-02     21          3.85
>PR

PR   8  2.00  E-02   D  2.00  E-02     21         12
>PR

PR   8  2.00  E-02   D  2.00  E-02     21         12.4
>PR

PR   8  2.00  E-02   D  2.00  E-02     21         14.5
>
?
>PR

PR   8  2.00  E-02   D  2.00  E-02     21         28.8
>PR

PR   8  2.00  E-02   D  2.00  E-02     21         35.8
>PR

PR   8  2.00  E-02   D  2.00  E-02     21         36
>PR

PR   8  2.00  E-02   D  2.00  E-02     21         39.6
>PR

PR   8  2.00  E-02   D  2.00  E-02     21         40.1
>PR

PR   8  2.00  E-02   D  2.00  E-02     21         41.5
>PR

PR   8  2.00  E-02   D  2.00  E-02     21         44.4
>PR

PR   8  2.00  E-02   D  2.00  E-02     21         48.3
>PRPR

PR   8  2.00  E-02   D  2.00  E-02     21         49.4
>PR

PR   8  2.00  E-02   D  2.00  E-02     21         51.4
>PR

PR   8  2.00  E-02   D  2.00  E-02     21         52.5
>PR

PR   8  2.00  E-02   D  2.00  E-02     21         53
>PR
```

TABLE XXXXV. DWELL TEST NO. 17 (CONT'D)

```
PR  8 2.00 E-02  D 2.00 E-02    21           53.1
>PR

PR  8 2.00 E-02  D 2.00 E-02    21           54.7
>PR

PR  8 2.00 E-02  D 2.00 E-02    21           55.9
>PRP

PR  8 2.00 E-02  D 2.00 E-02    21           57.4
>PR

PR  8 2.00 E-02  D 2.00 E-02    21           58.4
>
?
>PR

PR  8 2.00 E-02  D 2.00 E-02    21           62
>
*MANUAL ABORT*
AB 8 2.00 E-02  D 2.00 E-02    21          62
>
```

Dwell at 42 Hz for 1 hr.

```
>
UP  8 2.95 E-03  D 2.99 E-03    42            0
>PR

PR  8 2.98 E-03  D 2.99 E-03    42            4.09
>PR

PR  8 2.98 E-03  D 2.99 E-03    42            6.33
>PR

PR  8 2.99 E-03  D 2.99 E-03    42           11.9
>PRPR

PR  8 2.99 E-03  D 2.99 E-03    42           14.6
>PRPR

PR  8 2.99 E-03  D 2.99 E-03    42           24.7
>PR

PR  8 2.99 E-03  D 2.99 E-03    42           38.1
>PR

PR  8 2.99 E-03  D 2.99 E-03    42           38.3
>PR

PR  8 2.99 E-03  D 2.99 E-03    42           46.7
>PRPR

PR  8 2.99 E-03  D 2.99 E-03    42           52.5
>PR
```

TABLE XXXXV. DWELL TEST NO. 17 (CONT'D)

```
PR  8 2.98 E-03  D 2.99 E-03    42        52.6
>PR

PR  8 2.98 E-03  D 2.99 E-03    42        55.9
>PR

PR  8 2.98 E-03  D 2.99 E-03    42        58
>PR

PR  8 2.99 E-03  D 2.99 E-03    42        58.3
>PR

PR  8 2.98 E-03  D 2.99 E-03    42        58.3
>PRPR

PR  8 2.99 E-03  D 2.99 E-03    42        59
>PR

PR  8 2.99 E-03  D 2.99 E-03    42        59
>PR

PR  8 2.99 E-03  D 2.99 E-03    42        59.1
>PR

PR  8 2.98 E-03  D 2.99 E-03    42        59.7
>PR

PR  8 2.98 E-03  D 2.99 E-03    42        59.7
>PR

PR  8 2.99 E-03  D 2.99 E-03    42        60
>
*MANUAL ABORT*
AB 8 2.93 E-03  D 2.99 E-03    42        60.1
>
*MANUAL ABORT*
AB 8      0     D 2.99 E-03    42        60.1
>
```

Dwell at 7.5 Hz for 1 hr.

```
 HO
>
UP  8 3.06 E-02  D 3.00 E-02     7.5        0
>PR

PR  8 3.00 E-02  D 3.00 E-02     7.5        5.72
>PR

PR  8 3.02 E-02  D 3.00 E-02     7.5        8.84
>
?
>PR

PR  8 2.97 E-02  D 3.00 E-02     7.5       15.2
>PRPR
```

TABLE XXXXV. DWELL TEST NO. 17 (CONT'D)

```
PR  S 2.97 E-02  D 3.00 E-02     7.5       15.9
>PR

PR  S 2.97 E-02  D 3.00 E-02     7.5       18.6
>
?
>PR

PR  S 3.02 E-02  D 3.00 E-02     7.5       22.9
>PR

PR  S 2.97 E-02  D 3.00 E-02     7.5       30.9
>PR

PR  S 2.99 E-02  D 3.00 E-02     7.5       36.1
>PR

PR  S 3.00 E-02  D 3.00 E-02     7.5       46.3
>PR

PR  S 2.97 E-02  D 3.00 E-02     7.5       54.5
>
AL  S 2.42 E-02  D 3.00 E-02     7.5       55.1
>PR

PR  S 3.04 E-02  D 3.00 E-02     7.5       55.5
>PR

PR  S 2.94 E-02  D 3.00 E-02     7.5       57.7
>PRPR

PR  S 2.98 E-02  D 3.00 E-02     7.5       59
>
*MANUAL ABORT*
AB S 2.96 E-02  D 3.00 E-02     7.5       59.7
>
```

TABLE XXXXVI. DWELL TEST NO. 20

Dwell at 21 Hz for 15 min

```
 40
>
UP  S 6.02 E-02  D 6.02 E-02     21          0
>PR

PR  S 6.01 E-02  D 6.02 E-02     21          3.25
>PR

PR  S 6.02 E-02  D 6.02 E-02     21          3.38
>PR

PR  S 6.01 E-02  D 6.02 E-02     21          3.5
>PR

PR  S 6.02 E-02  D 6.02 E-02     21          3.69
>PR
```

```
PR  8 6.01 E-02  D 6.02 E-02    21          4.83
> PR
?
>PR

PR  8 6.01 E-02  D 6.02 E-02    21          8.34
>PR

PR  8 6.02 E-02  D 6.02 E-02    21         13.9
>PR

PR  8 6.01 E-02  D 6.02 E-02    21         14.7
>PR

PR  8 6.02 E-02  D 6.02 E-02    21         14.8
>
?
>
*MANUAL ABORT*
AB 8 6.01 E-02  D 6.02 E-02    21         15.1
>
```

Dwell at 60 Hz for 15 min

```
 40

>
UP  8 5.81 E-02  D 6.02 E-02    60          0
>PR

PR  8 6.01 E-02  D 6.02 E-02    60          4.27
>PR

PR  8 6.01 E-02  D 6.02 E-02    60          4.48
>PR

PR  8 6.01 E-02  D 6.02 E-02    60          4.70
>
*MANUAL ABORT*
AB 8 6.02 E-02  D 6.02 E-02    60         15.3
>
```

TABLE XXXXVII. TOTAL PRETEST PROGRAMMING SETUP TIME

Test No.	Test ID	Feedin editor/compiler tape (min) ①	List data tape (min-sec) ②	Edit list data tape (min) ③	Feedin sine operating tape (min) ④	Read in new data tape (sec) ⑤	Total setup time with no previous preparations (min) ⑥	Total setup time for repeated testing* (min) ⑦	Total setup time for repeated testing when all tapes are disc stored* (min) ⑧
1	MIL-STD-810B, Fig 514.1-1-Z	2.5	2 - 40	10.70	4.0	8	17.35	4.15	Under 1.0
2	MIL-STD-810B, Fig 514.1-1-B	"	2 - 45	10.75	"	8	17.40		
3	MIL-STD-810B Fig 514.1-2-C	"	3 - 25	11.40	"	9	18.10		
4	MIL-STD-810B Fig 514.1-2-H	"	3 - 22	11.40	"	10	18.10		
5	MIL-STD-810B Fig 514.1-2-L	"	3 - 24	11.40	"	10	18.10		
6	MIL-STD-810B Fig 514.1-3-M	"	3 - 22	11.40	"	9	18.10		
7	MIL-STD-810B Fig 514.1-4-C	"	3 - 22	11.40	"	9	18.10		
8	MIL-STD-810B Fig 514.1-4-H	"	3 - 25	11.40	"	10	18.10		
9	MIL-STD-810B Fig 514.1-4-AR	"	2 - 44	10.75	"	8	17.40		
10	MIL-STD-810B Fig 514.1-4-N	"	3 - 19	11.30	"	9	17.95		
11	MIL-STD-810B Fig 514.1-5-P	"	3 - 19	11.30	"	10	17.95		
12	MIL-STD-810B Fig 514.1-5-U	"	3 - 18	11.30	"	9	17.95		
13	MIL-STD-810B Fig 514.1-6-V	"	3 - 4	11.0	"	9	17.65		
14	MIL-STD-810B Fig 514.1-6-W	"	3 - 5	11.0	"	9	17.65		
15	MIL-STD-810B Fig 514.1-7-AX	"	3 - 19	11.30	"	9	17.95		
16	MIL-STD-810B Fig 514.1-7-AV	"	3 - 19	11.30	"	10	17.95		
17	MIL-STD-167	"	2 - 44	10.75	"	10	17.40		
18	MIL-STD-331 Test 104 5.1.2.1	"	2 - 20	10.35	"	8	17.00		
19	MIL-STD-331 Test 104 5.2.1.1	"	2 - 18	10.30	"	9	16.95		
20	MIL-STD-331 Test 114 5.2.1	"	2 - 22	10.35	"	9	17.00		
21	MIL-STD-810C - A	"	2 - 43	10.75	"	9	17.40		
22	MIL-STD-810C - B	"	3 - 17	11.30	"	9	17.95		
23	MIL-STD-810C - C	"	3 - 16	11.25	"	8.8	17.90		

AVERAGE = 17.75 min   AVERAGE = 4.15 min   AVERAGE = <1.0 min

77-percent Improvement   76-percent Improvement

95-percent Improvement

T_n = Denotes time

Note: (1) $T_{⑥} = T_{①} + \sum_{n=①}^{⑤} T_{ⓝ}$

$T_{⑦} = T_{⑥} + T_{⑤}$

T_8 = Estimated computer/disc internal transfer time (ultimate operating condition)

(2) Data in column 2 contain an average of 8.0 min allotted for the EDIT (test-data tape preparation) routine.

* - Applicable only to second test and subsequents

(3) Improvement in setup time = $100 \left[1 - \frac{T_{n_1}}{T_{n_2}}\right]$ percent

Where T_{n_1} and T_{n_2} are any two-time datum.

TABLE XXXXVIII. LIMIT PERFORMANCE SINE TESTS/T5021 SYSTEM AND C90 EXCITER

Test Level	Frequency (Hz)	Mode*	Amplitude	Equiv accel (g)	Time (min)	Sweep rate (oct/min)	Sweep cycles (cyl)	Remarks
1	5-30	D	.53	(7/25)				Test configuration shall include:
2	300-125	D	.13	(6/101)				Mass Specimen = 15
3	125-225	V	30.0	(61/110)				ABORT Limits = ±1.0 dB
4	225-300	A	120.0	(120)				ALARM Limits = ±0.5 dB
5	300-750	A	80.0	(80)				Q = Low <50.0
6	750-1500	D	.0010	(29/115)				
7	1500-2000	A	120.0	(120)				A = Accel in g's, 1 g = 386.0 in./sec^2
8	2000-2300	V	3.0	(97/112)				V = Velocity in in./sec
9	2300-2450	A	40.0	(40)				
10	2450-3000	A	120.0	(120)	10.0		2.0	D = Displacement in inch-double amplitude
1-10	Same as above					7.0	1.0	Note:
1-10	" " "				10	0.1**		$\ddot{X} = 5.12 \times 10^{-2}$ $(XW^2) \sim$ g's
1-10	" " "				60.0	7.0		$\ddot{X} = 1.63 \times 10^{-2}$ $(\dot{X}W) \sim$ g's
1-10	" " "				480.0	0.1		$X \equiv D$, $\dot{X} = V$
1	150-151	A	100.0	(100)				
2	152-153	V	50.0	(120)				
3	153-154	D	.075	(85)	4.26	0.1		

*See Remarks column
**In Y plane

10.8 State-of-the-Art Developments in Direct-Digital Control of Dynamic Testing

10.8.1 Manufacturers

The primary manufacturers/designers of digitally-controlled vibration test systems include:

(a) Gilmore Industries/MB Electronics - (Cleveland, Ohio)

(b) Hewlett-Packard Co - (Santa Clara, California)

(c) Ling Electronics - (Anaheim, California)

(d) Time/Data Corp - (Palo Alto, California)

Each manufacturer/designer supplies the necessary software to operate the DDC system. Some specialize as sole suppliers of the complete control/test system, which includes the entire electronics as well as the shaker and power amplifier; others provide the digital-control system only, which is subsequently interfaced with the customer's specific shaker and power amplifier. Most manufacturer's supplying the control system only will perform the interface work when requested by the customer.

10.8.2 Software Developments

The standard digital control software routines offered by the industry permit the following tests:

(1) Multiple-level acceleration, velocity, or displacement modes for sine-sweep tests over a wide frequency band (typically 5 to 3000 Hz) at sweep speeds typically varying between 0.1 and 10.0 octaves/min.* Amplitude-control limits can be set at as low as ±0.5 dB (approx ±0.5 percent) and as high as ±50.0 dB. A manual ABORT feature enables the operator to execute real-time amplitude modification at selective frequency bands. The sine-sweep routine can be used to perform any tests specified in MIL-STD-810B and 331 or MIL-STD-167, and is flexible enough to permit the execution of any existing arbitrary sine-sweep test, within the electromechanical limitation of the test system.

(2) Random vibration tests that enable the user to specify selectable frequency bands, amplitude profiles in terms of g^2/Hz, or g rms using straight lines interpolation, and selectable filter resolutions, typically set at 64, 128, 256 or 512 lines. The number of profile points is limited (typically to 10 lines) and permits entries of positive and negative slopes expressed in ±dB/octave. The net result is that

---

**sweep speeds as high as 33 octaves/min for a total of 32 programmable test levels currently under development.*

a complex PSD spectra can be adequately specified over the frequency band of 5 to 5000 Hz where the bulk of the military and mechanical test work is performed. Here too, the existing software is in good compliance with the test-spectra requirements specified in MIL-STD-810B. The PSD spectrum control accuracy could be specified to well within the required ±1.5 to ±3.0 dB, depending on frequency.

The software will usually permit the operator to calculate the rms and peak acceleration levels associated with the specified PSD spectra. A main feature of the random routine is its ability to equalize to the specified spectra within seconds, as well as to automatically compensate for the shaker/specimen dynamic interactions based on internally programmed transfer function routines.

(3) The standard analysis routine offered enables the user to compute the PSD spectra, the g rms, and Fourier time series representation of an externally supplied analog signal. Normally, this routine is used in the analysis of a complex pulse and at the completion of the test, as insufficient core capacity may preclude real-time processing. It is also physically impossible to simultaneously printout the test PSD spectra, and the time series analysis using a single teleprinter.

Nonstandard software routines are, of course, custom tailored to specific applications. Such development may include a mixed sine/random test where a sweep-sine test is simultaneously superimposed on a PSD spectrum, or a sine/shock test where the shaker can be excited for a specific number of cycles at selective frequencies only. Further advancement includes a multishaker sine-sweep control routine where a large platform supported by several shakers can be controlled in both phase and amplitude by a single-source digital controller.

Software for multichannel amplitude control techniques have already been developed. At this operating mode, data from up to eight feedback channels are statistically analyzed and weighed according to a desired control preference. These channels supply data from accelerometers placed at selected points of interest within the test package.

10.8.3 Future Developments In Software Routines

These routines include:

(1) Shock spectrum programs that permit the operator to electronically duplicate the specified shock spectrum for various values of damping factors. Here too, the routine will automatically compensate for any shaker/specimen dynamic interactions, with the net result that specified spectra are satisfied at acceptable percent errors. Selective band spectra modifications are also possible.

(2) Routines to generate simple or complex acceleration-time histories. This case is an extension of item (1) above and can be extracted from FFT techniques by proper software instructions. If perfected, it could become extremely useful in simulating a variety of

true field environments in the test laboratory. Time transients will be generated electronically, practically eliminating the need for trial pulses.

In this regard, the most natural way of simulating shock environment for any test specimen is, of course, the accurate reconstruction of the acceleration time history as experienced in the field.

(3) Resonance search and dwell sine-sweep routines that will enable the operator to specify a test envelope within which the system will automatically search for a specified amplification with respect to a defined input. When the sweep cycle is completed, the test system will automatically adjust itself to the frequencies at which resonance was determined, and dwell for a specified time in each frequency.

(4) Mobility testing routine for structural model analysis.

ACKNOWLEDGEMENT

The author expresses his sincere appreciation to HDL staff members E. Smith, D. Bryant, and F. Nelson for their effort, dedication, and skill demonstrated during the test program. Their ingenuity resulted in solutions to numerous real-time problems. Assistance rendered by M. Needleman in analyzing the test data is also highly valued.

LITERATURE CITED

(1) Sine-Test Electrodynamic Vibration Systems Using Digital Control - F.C. Bosso, Proceedings of the Institute of Environmental Sciences, 16th Annual Meeting, Boston, April 1970.

(2) Digitally Controlled Sweep Servo Oscillator - R.L. Reiner, MB Electronics, Proceedings of the Institute of Environmental Sciences, 16th Annual Meeting, Boston, April 1970.

(3) Digital Control Systems for Electrodynamic Vibration Exciters - Alfred G. Ratz, Proceedings 16th Annual International Symposium on Aerospace Instrumentation, Seattle, May 11-13, 1970.

(4) T5021 Sine/Random Vibration System Operating Manual - MB Electronics/Gilmore Industries.

(5) Shock Testing Utilizing A Time Sharing Digital Computer - Robert W. Canon, Naval Missile Center, Point Mugu, California.

(6) Sampled Data Reconstruction Errors - John V. Wait, University of Arizona (Instrument & Control System - June 1970).

DISTRIBUTION

DEFENSE METALS INFORMATION CENTER
BATTELLE MEMORIAL INSTITUTE
505 KING AVENUE
COLUMBUS, OH 43201 (2 CY)

COMMANDER
DEFENSE DOCUMENTATION CENTER
CAMERON STATION
ALEXANDRIA, VA 22314
ATTN DDC-TCA (12 CY)

COMMANDER
U.S. ARMY FOREIGN SCIENCE AND TECHNOLOGY CTR
SEVENTH STREET, NE
CHARLOTTESVILLE, VA 22901
ATTN AMXST-SD3, 220

OFFICE OF CHIEF OF RESEARCH AND DEVELOPMENT
DEPARTMENT OF THE ARMY
WASHINGTON, DC 20310
ATTN DARD-ARS-P

COMMANDER
ARMY RESEARCH OFFICE
BOX CM
DUKE STATION
DURHAM, NC 27706
ATTN DR. H.M. DAVIS
ATTN J.J. MURRAY

COMMANDER
U.S. ARMY MATERIEL COMMAND
ALEXANDRIA, VA 22304
ATTN AMCQA-V
ATTN AMCQA-P
ATTN AMCQA-E
ATTN AMCRD-TC
ATTN AMCDL
ATTN AMCRD-EA
ATTN AMCRD-U

COMMANDER
U.S. ARMY ELECTRONICS COMMAND
FORT MONMOUTH, NJ 07703
ATTN AMSEL-PA-P
ATTN AMSEL-CT-DT
ATTN AMSEL-TL-DT
ATTN AMSEL-WL-DO
ATTN AMSEL-Vl-D
ATTN AMSEL-RD-EA

COMMANDER
USA AIR MOBILITY RESEARCH & DEVELOPMENT LAB
MOFFET FIELD, CA 94035
ATTN TECHNICAL DIRECTOR
ATTN CHIEF, VIBRATION TEST LAB

COMMANDER
PACIFIC MISSILE RANGE
NAVAL MISSILE CENTER
POINT MUGU, CA 93042
ATTN CHIEF, VIBRATION TEST LAB

COMMANDER
NAVAL ELECTRONICS LABORATORY CENTER
SAN DIEGO, CA 92152
ATTN CHIEF, VIBRATION TEST LAB

COMMANDING OFFICER
NAVAL CIVIL ENGINEERING LABORATORY
PORT HUENEME, CA 93043
ATTN CHIEF, VIBRATION TEST LAB

COMMANDER
NAVAL UNDERSEA CENTER
SAN DIEGO, CA 92132
ATTN CHIEF, VIBRATION TEST LAB

COMMANDER
U.S. ARMY MISSILE COMMAND
REDSTONE ARSENAL, AL 35809
ATTN AMSMI-RP, REDSTONE SCIENTIFIC INFORMATION CTR (2 CY)
ATTN AMSMI-RKC, MR J. ALLEY
ATTN ANSMI-M
ATTN AMSMI-Q, MR. ROBERT O. BLACK
ATTN AMSMI-QS MR. GEORGE L. STEWART, JR.
ATTN AMSMI-QSD MR. LESLIE CONGER

COMMANDER
U.S. ARMY TROOP SUPPORT COMMAND
4300 GOODFELLOW BOULEVARD
ST. LOUIS, MO 63120
ATTN AMSTS-QR
ATTN AMSTS-M
ATTN AMSTS-P
ATTN AMSTS-R

COMMANDER
U.S. ARMY NATICK LABORATORIES
KANSAS STREET
NATICK, MA 01760
ATTN STSNLT-EQR
ATTN STSNLT-GE

COMMANDER
U.S. ARMY MOBILITY EQUIPMENT RESEARCH & DEV CTR
FORT BELVOIR, VA 22060 (2 CY)
ATTN STSFB-E
ATTN STSFB-M
ATTN STSFB-MM
ATTN STSFB-CL
ATTN STSFB-X
ATTN STSFB-D
ATTN STSFB-DQ
ATTN STSFB-O
ATTN STSFB-J
ATTN STSFB-W

COMMANDER
U.S. ARMY TANK-AUTOMOTIVE COMMAND
28251 VAN DYKE AVENUE
WARREN, MI 48090
ATTN AMSTA-RKA MR J. DUDZINSKI
ATTN AMSTA-RKA MR. W. WULF
ATTN AMSTA-RHP MR. O. RENIUS
ATTN AMSTA-QE MR. P. DUIKA
ATTN AMSTA-RKC MR. CHARLES GREEN

COMMANDER
U.S. ARMY ARMAMENT COMMAND
ROCK ISLAND, IL 61201
ATTN AMSAR-QA (2 CY)
ATTN AMSAR-SC
ATTN AMSAR-RDP
ATTN AMSAR-EN

COMMANDER
EDGEWOOD ARSENAL
ABERDEEN PROVING GROUND, MD 21010
ATTN SAREA-TS-A
ATTN SAREA-PA-Q
ATTN SAREA-PA-T

COMMANDER
FRANKFORD ARSENAL
PHILADELPHIA, PA 19137
ATTN SARFA-TD
ATTN SARFA-TSE (2 CY)
ATTN SARFA-FC
ATTN SARFA-MD
ATTN SARFA-PD
ATTN SARFA-QA

COMMANDER
PICATINNY ARSENAL
DOVER, NJ 07801
ATTN SARPA-TS-S MR. M. COSTELLO
ATTN SARPA-FR-P MR. H. DEFAZIO
ATTN SARPA-FR-S MR. T.M. ROACH, JR
ATTN SARPA-FR-G MR. A.J. CLEAR
ATTN SARPA-QA-T MR. D. STEIN
ATTN SARPA-FR-M MR. W. POWERS
ATTN TECHNICAL DIRECTOR
ATTN A. MENDIS
ATTN SARPA-DC7 (MIL-STD-331 SPECIFICATIONS COMMITTEE)

COMMANDER
ROCK ISLAND ARSENAL
ROCK ISLAND, IL 61201
ATTN SARRI-L DR. BECKETT
ATTN SARRI-LEQ MR. J. HAUSMAN
ATTN SARRI-LR MR. W. KISNER (2 CY)
ATTN SARRI-Q MR. W. BETTS
ATTN SARRI-RS MR. V. LONG
ATTN SARRI-LR MR. W. MCHENRY

COMMANDER
WATERVLIET ARSENAL
WATERVLIET, NY 12189 (2 CY)
ATTN SARWV-PPI MR. L.A. JETTE
ATTN SARWV-RDS MR. M.L. SLAWSKY
ATTN SARWV-RDR DR. F.W. SCHMEIDESHOFF
ATTN SARWV-QA MR. J.J. MILLER
ATTN SARWV-QA QUALITY ASSURANCE DIRECTORATE

COMMANDER
U.S. ARMY AVIATION SYSTEMS COMMAND
ST. LOUIS, MO 63166
ATTN AMSAV-EE
ATTN AMSAV-EEG
ATTN AMSAV-FEE
ATTN AMSAV-LE
ATTN AMSAV-LEP
ATTN AMSAV-LSA
ATTN AMSAV-PV
ATTN AMSAV-EFS

COMMANDER
U.S. ARMY AERONAUTICAL DEPOT MAINTENANCE CENTER
(MAIL STOP 55)
CORPUS CHRISTI, TX 78419
ATTN AMSAV-FES MR. BEE

DIRECTOR
U.S. ARMY PRODUCTION EQUIPMENT AGENCY
ROCK ISLAND ARSENAL
ROCK ISLAND, IL 61201
ATTN AMXPE-MT

COMMANDER
U.S. ARMY TEST & EVALUATION COMMAND
ABERDEEN PROVING GROUND, MD 21005
ATTN AMSTE-RA

COMMANDER
U.S. ARMY WHITE SANDS MISSILE RANGE
WSMR, NM 88002
ATTN STEWS-AD-L
ATTN STEWS-ID-P
ATTN F. EDGINTON-TE-AD
ATTN D. SCHAEPEN-STEWS-TE-MF

COMMANDER
U.S. ARMY YUMA PROVING GROUND
YUMA, AZ 85364
ATTN STEYP-MTS
ATTN STEYP-ADT

COMMANDER
U.S. ARMY TROPIC TEST CENTER
FT. CLAYTON, CZ
ATTN STETC-XO-A, DRAWER 942

COMMANDER
ABERDEEN PROVING GROUND, MD 21005
ATTN STEAP-MT
ATTN STEAP-TL
ATTN STEAP-MT-M MR. J.A. FEROLI
ATTN STEAP-MT-G MR. R.L. HUDDLESTON

COMMANDER
U.S. ARMY ARCTIC TEST CENTER
APO SEATTLE 98733
ATTN STEAC-MO-AS

COMMANDER
DUGWAY PROVING GROUND
UTAH 84022
ATTN STEPD-TO(D)

COMMANDER
U.S. ARMY ELECTRONIC PROVING GROUND
FT HUACHUCA, AZ 85613
ATTN STEEP-MT

COMMANDER
JEFFERSON PROVING GROUND
MADISON, IN 47250
ATTN STEJP-TD-I

PRESIDENT
U.S. ARMY AIRBORNE
COMMUNICATIONS & ELECTRONICS BOARD
FT. BRAGG, NC 28307
ATTN STEBF-TD

PRESIDENT
U.S. ARMY AIR DEFENSE BOARD
FT BLISS, TX 79916
ATTN STEBD-TD

PRESIDENT
U.S. ARMY ARMOR & ENGINEER BOARD
FT KNOX, KY 40121
ATTN STEBB-TD

PRESIDENT
U.S. ARMY AVIATION TEST BOARD
FT RUCKER, AL 36360
ATTN STEBG-MT

PRESIDENT
U.S. ARMY FIELD ARTILLERY BOARD
FT SILL, OK 73503
ATTN STEBA-TD

PRESIDENT
U.S. ARMY INFANTRY BOARD
FT BENNING, GA 31905
ATTN STEBC-TE

COMMANDER
ANNISTON ARMY DEPOT
ANNISTON, AL 36202
ATTN AMXAN-QA

COMMANDER
LETTERKENNY ARMY DEPOT
CHAMBERSBURG, PA 17201
ATTN AMXLE-QA 17201

COMMANDER
LEXINGTON-BLUEGRASS ARMY DEPOT
LEXINGTON, KY 40507
ATTN AMXLX-QA

COMMANDER
NEW CUMBERLAND ARMY DEPOT
NEW CUMBERLAND, PA 17070
ATTN AMXNC-QA

COMMANDER
PUEBLO ARMY DEPOT
PUEBLO, CO 81001
ATTN AMXPU-Q (2 CY)

COMMANDER
RED RIVER ARMY DEPOT
TEXARKANA, TX 75501
ATTN AMXRR-QA

COMMANDER
SACREMENTO ARMY DEPOT
SACREMENTO, CA 95801
ATTN AMXSA-QA

COMMANDER
SAVANNA ARMY DEPOT
SAVANNA, IL 61074
ATTN AMXSV-QA

DIRECTOR
AMC AMMUNICATION CENTER
SAVANNA, IL 61074
ATTN AMXAC-DE

COMMANDER
SENECA ARMY DEPOT
ROMULUS, NY 14541
ATTN AMXSE-RG

COMMANDER
SHARPE ARMY DEPOT
LATHROP, CA 95330
ATTN AMXSH-QE

COMMANDER
SIERRA ARMY DEPOT
HERLONG, CA 96113
ATTN AMXSI-DQA

COMMANDER
TOBYHANNA ARMY DEPOT
TOBYHANNA, PA 18466
ATTN AMXTO-Q

COMMANDER
TOOELE ARMY DEPOT
TOOELE, UT 84074
ATTN AMXTE-QA (2 CY)

CHIEF
BUREAU OF NAVAL WEAPONS
DEPARTMENT OF THE NAVY
WASHINGTON, DC 20390

CHIEF
BUREAU OF SHIPS
DEPARTMENT OF THE NAVY
WASHINGTON, DC 20315

COMMANDER
WRIGHT AIR DEVELOPMENT DIVISION
WRIGHT-PATTERSON AFB, OH 45433
ATTN ASRC (2 CY)
ATTN D. EARLS

DIRECTOR
AIR FORCE MATERIEL LABORATORY
WRIGHT-PATTERSON AFB, OH 45433
ATTN AFML-DO-LIBRARY

DIRECTOR
ARMY MATERIALS AND MECHANICS CENTER
WATERTOWN, MA 02172
ATTN AMXMR-PL (2 CY)
ATTN AMXMR-M
ATTN AMXMR-P
ATTN AMXMR-RA MR. F. VALENTE
ATTN AMXMR-MQ (2 CY)
ATTN AMXMR-MS
ATTN AMXMR-MI MR. H. HATCH

NASA, GODDARD SPACE FLIGHT CENTER
GREENBELT, MD 20771
ATTN B. KEEGAN
ATTN E.J. KIRTCHMAN
ATTN W.F. BANGS

DEPARTMENT OF COMMERCE
NATIONAL BUREAU OF STANDARDS
WASHINGTON, DC 20234
ATTN J.D. RAMBOZ

DIRECTOR
NAVAL RESEARCH LABORATORY
WASHINGTON, DC 20390
ATTN H.P USEY CODE 8404
ATTN H. FORKOIS CODE 8400
ATTN DR J.M. KRAFFT CODE 8430

COMMANDING OFFICER
NAVAL SURFACE WEAPONS CENTER
WHITE OAK, MD 20783
ATTN E.R. ZEPKA CODE 702
ATTN C.F. FRIEDINGER CODE 701
ATTN R.S. REED CODE 701

MCDONALD DOUGLAS CORPORATION
5301 BOLSA AVENUE
HUNTINGTON BEACH, CA 92647
ATTN M. BANGENTER

SANDIA LABORATORIES
LIVERMORE LABORATORY
P.O. BOX 969
LIVERMORE, CA 94550
ATTN D. B. NELSON

SANDIA LABORATORIES
P.O. BOX 5800
ALBERQUERQUE, NM 87115
ATTN D.O. SMALLWOOD
ATTN N. HUNTER

GRUMMAN AEROSPACE CORPORATION
SOUTH OYSTER BAY ROAD
BETHPAGE, NY 11714
ATTN CHIEF, VIBRATION TEST LABORATOR

JET PROPULSION LABORATORY
PASEDENA, CA
ATTN P. CHAPMAN

BOEING AEROSPACE CO
P.O. BOX 3999
SEATTLE, WA 98124
ATTN JOHN D. FAVOUR

HUGHES AIRCRAFT CO.
P.O. BOX 92919
LOS ANGELES, CA 90009
ATTN SHELDON RUBIN

KAMAN SCIENCES CORPORATION
P.O. BOX 7463
COLORADO SPRINGS, CO 80907
ATTN A.F. WITTE
ATTN F.J. WOLF

HARRY DIAMOND LABORATORIES
ATTN EINSEL, DAVID W., COL, COMMANDING OFFICER/FLYER, I.N./LANDIS, P.E./ CONRAD, E.E./SOMMER, H.
ATTN CARTER, W.W., DR., ACTING TECHNICAL DIRECTOR/MARCUS, S.M.
ATTN KIMMEL, S., PIO
ATTN CHIEF, 0021
ATTN CHIEF, 0022
ATTN CHIEF, LAB 400
ATTN CHIEF, LAB 500
ATTN CHIEF, LAB 600
ATTN CHIEF, DIV 700
ATTN CHIEF, DIV 800
ATTN CHIEF, LAB 900
ATTN CHIEF, LAB 1000
ATTN RECORD COPY, BR 041
ATTN HDL LIBRARY (3 CY)
ATTN CHAIRMAN, EDITORIAL COMMITTEE (4 CY)
ATTN CHIEF, 047
ATTN TECH REPORTS, 013
ATTN PATENT LAW BRANCH, 071
ATTN BIRD, F., 420
ATTN OVERMAN, D., 420
ATTN INGERSOL, P., 430
ATTN SHEBO, R., 530
ATTN EMMERMAN, P., 530
ATTN CRAWLEY, J., 610
ATTN NEILLY, D., 610
ATTN MCLAUGHLIN, P.W., 741
ATTN ANTEL, J., 750
ATTN WILLIS, B.F., 720
ATTN ZASTROW, K., 750
ATTN CHIEF 810
ATTN CHIEF 820
ATTN CHIEF 850
ATTN CURCHACK, H.D., 850
ATTN FRYDMAN, A.M., 850 (5 CY)
ATTN SMITH, E.R., 850
ATTN CHIEF 910
ATTN LUCEY, G., JR., 910
ATTN MEAD, O., SYSTEMS ANALYSIS
ATTN APOLENIS, C., DEPUTY CHIEF
ATTN CHIEF 420
ATTN CHIEF 430
ATTN CHIEF 610
ATTN CHIEF 530
ATTN CAMPAGNUOLO, C.J., 900
ATTN WYCKOFF, R.L., 700
ATTN ROSENHAFT, M., 722
ATTN YETTER, G., 750
ATTN SAMINSKY, H., 750

DEPARTMENT OF THE ARMY
HARRY DIAMOND LABORATORIES
2800 POWDER MILL RD
ADELPHI, MD 20783

OFFICIAL BUSINESS
PENALTY FOR PRIVATE USE $300

AN EQUAL OPPORTUNITY EMPLOYER

POSTAGE AND FEES PAID
DEPARTMENT OF THE ARMY
DOD 314

THIRD CLASS

COMMANDER
ROCK ISLAND ARSENAL
ROCK ISLAND, IL 61201

ATTN SARRI-L DR. BECKETT

Sarri-LPL

VANGUARD OF FREEDOM
BICENTENNIAL 1775-1975
UNITED STATES ARMY